SFQ-based on-chip digital readout for HPC-QC integration

HPCQC @CINECA, Italy – Dec 14th, 2023

Marco Arzeo, Lab manager at SEEQC-EU

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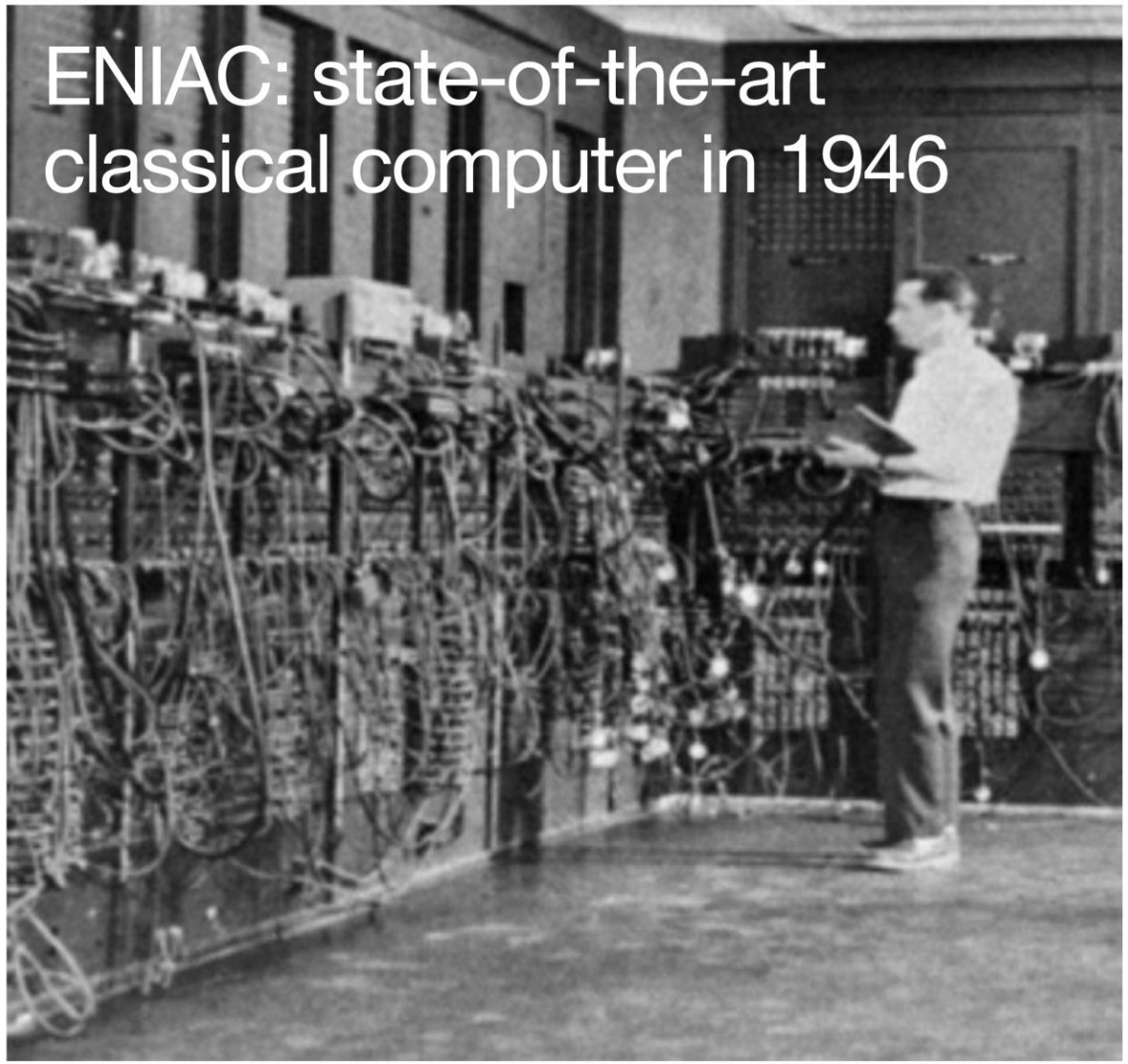
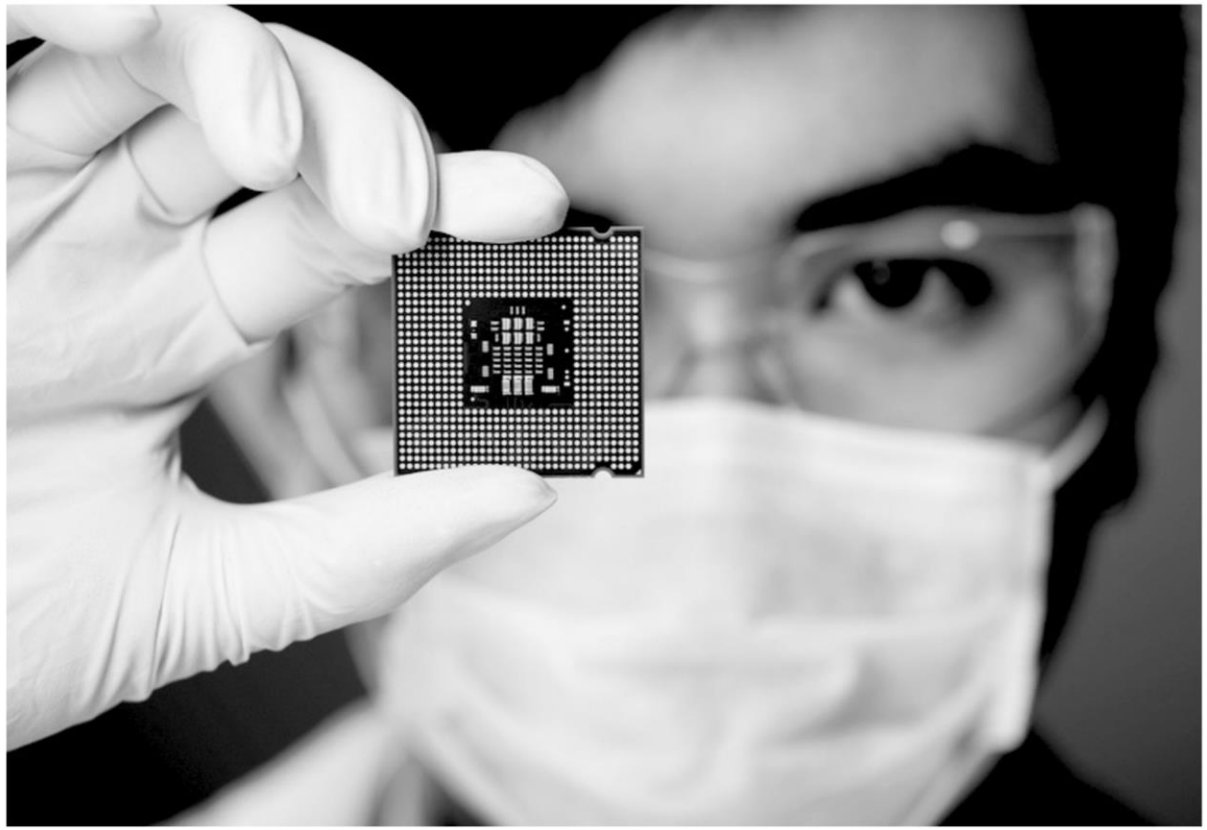


State-of-the-art CMOS chip



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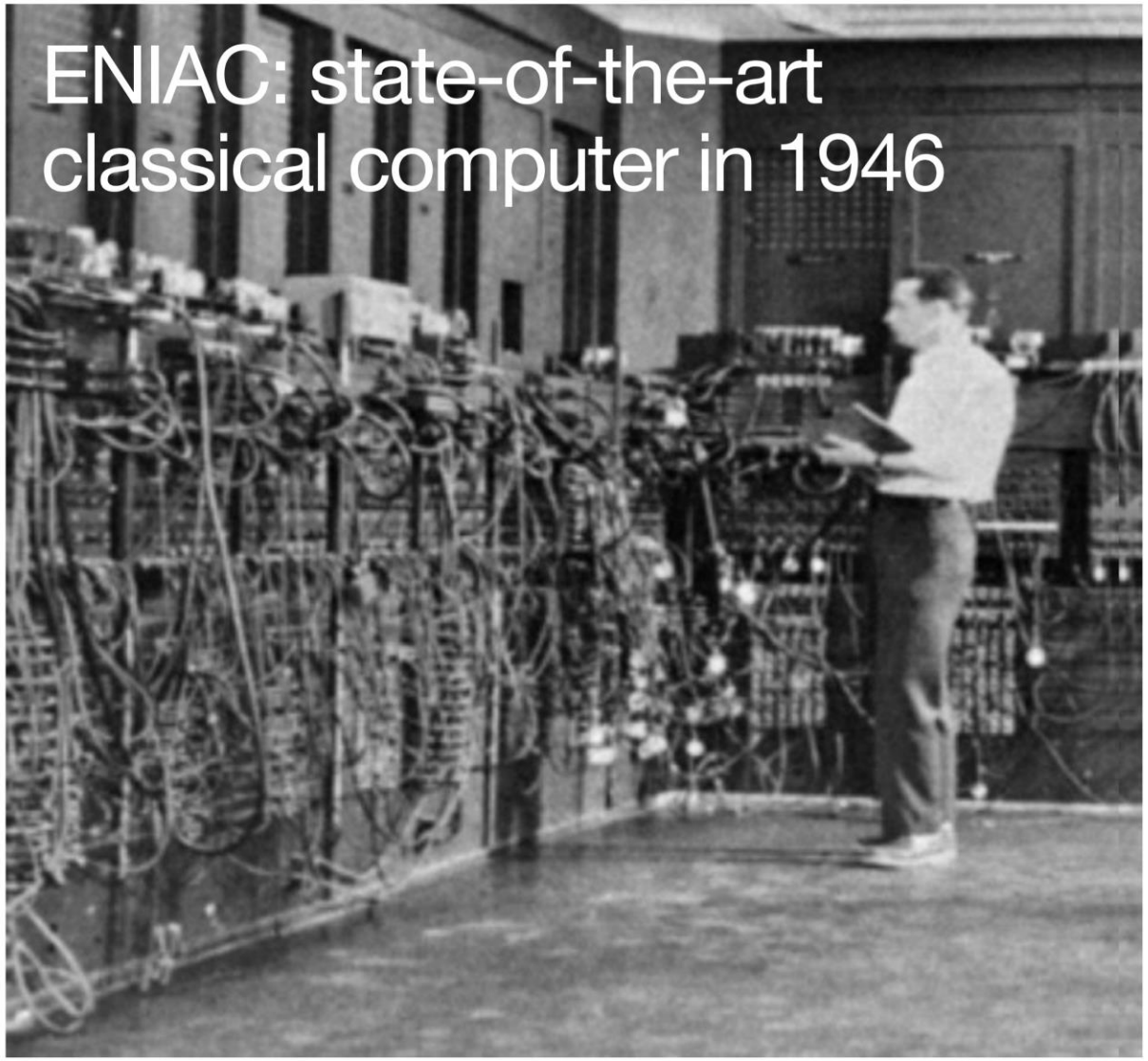
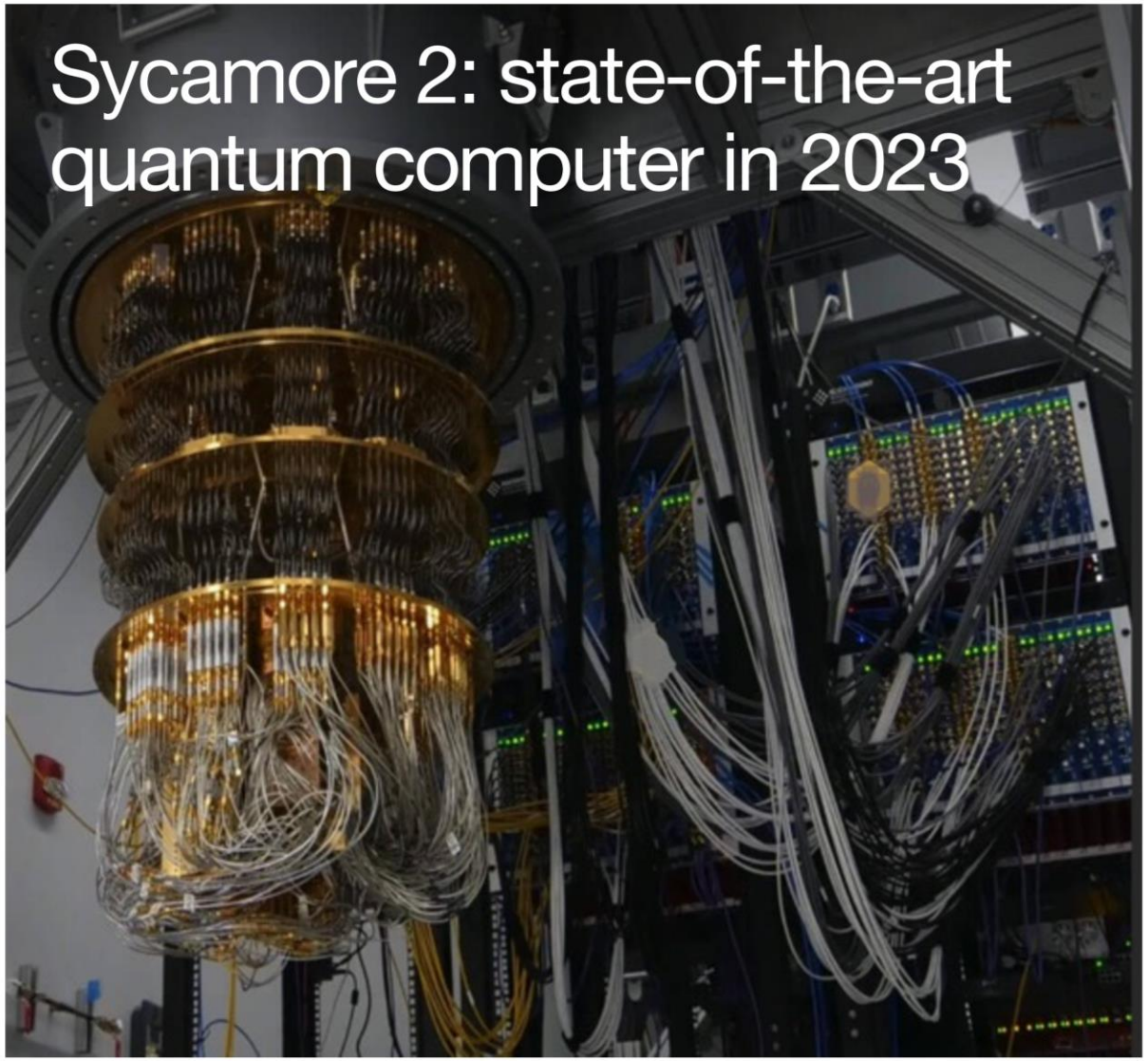
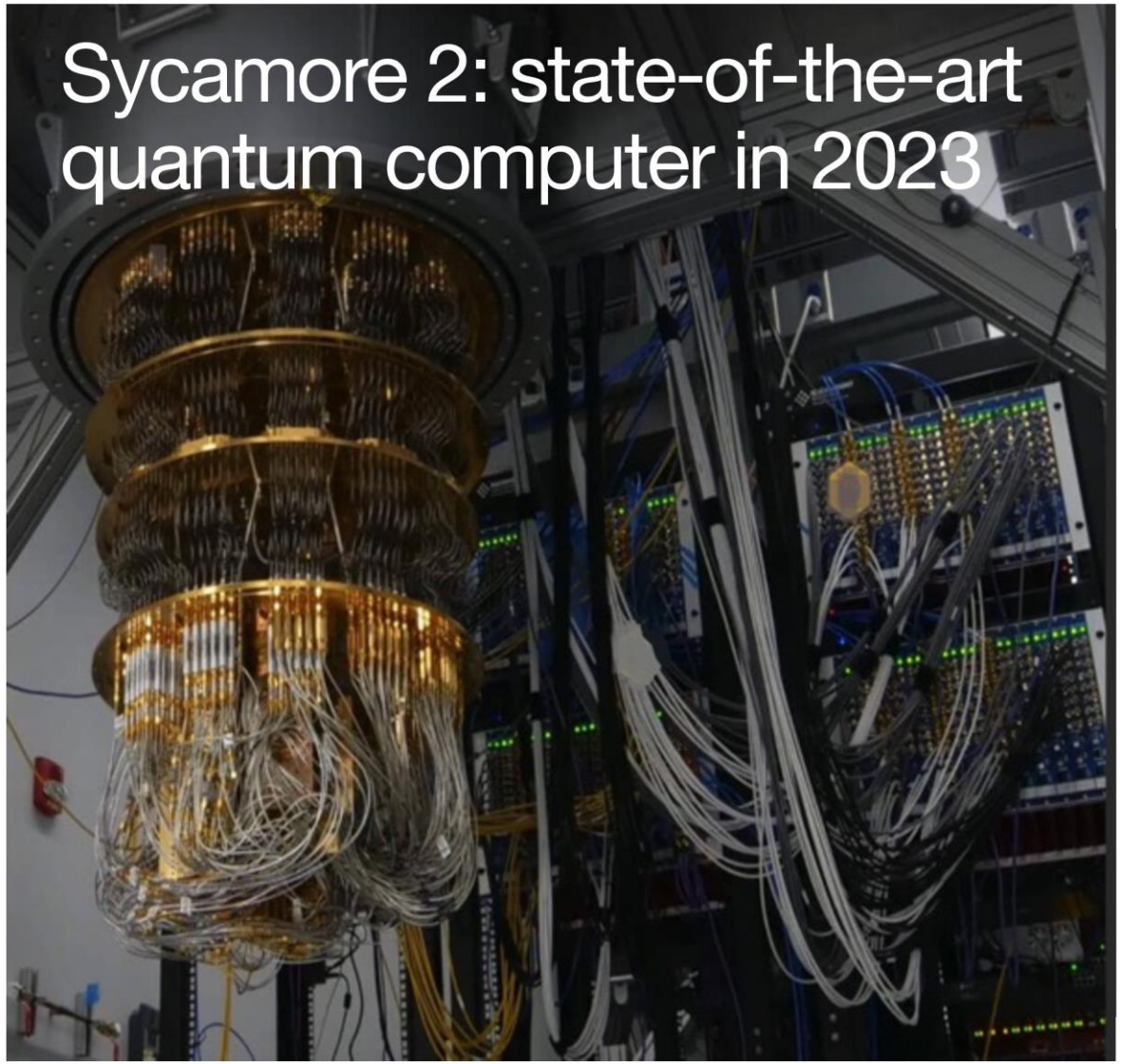
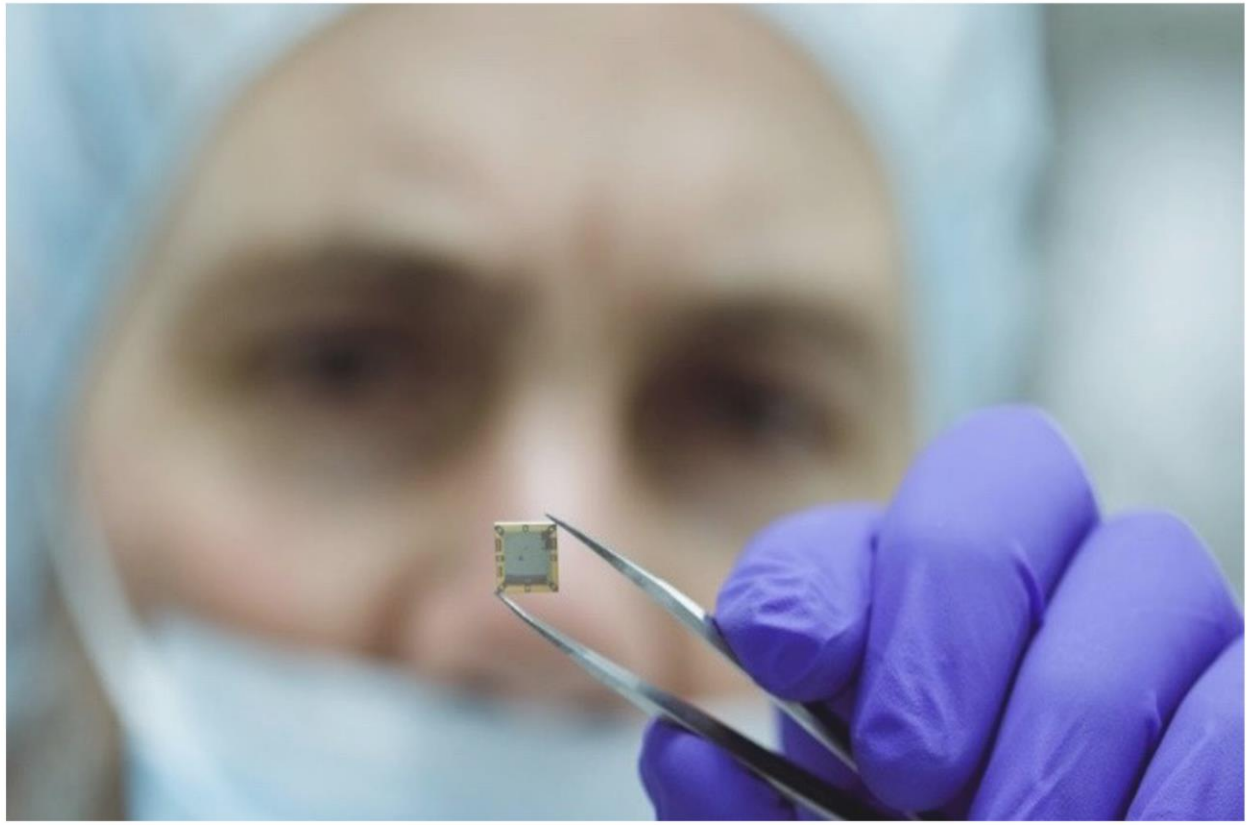

ENIAC: state-of-the-art
classical computer in 1946


Sycamore 2: state-of-the-art
quantum computer in 2023

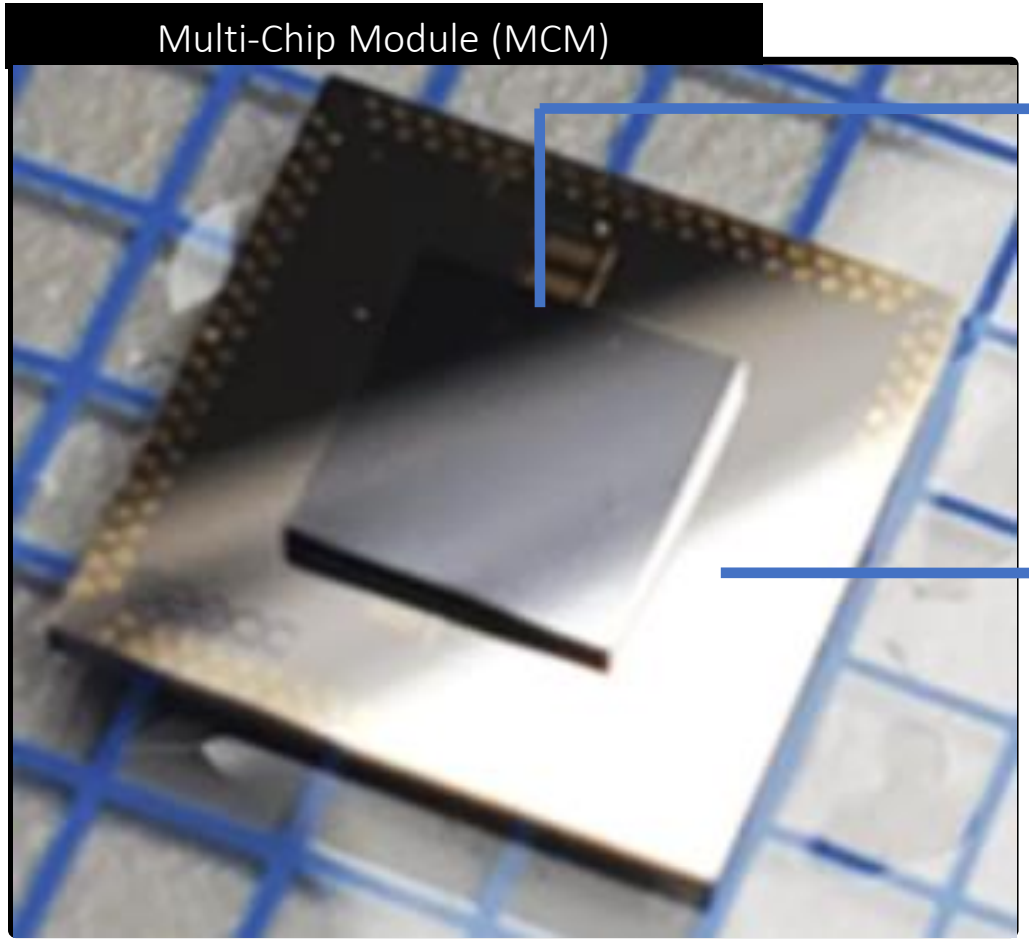
seeqc



State-of-the-art Single Flux Quantum (SFQ) chip



SEEQC – quantum computer on a chip

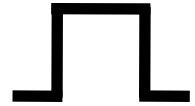


Qubit layer – compatible with all leading qubit technologies

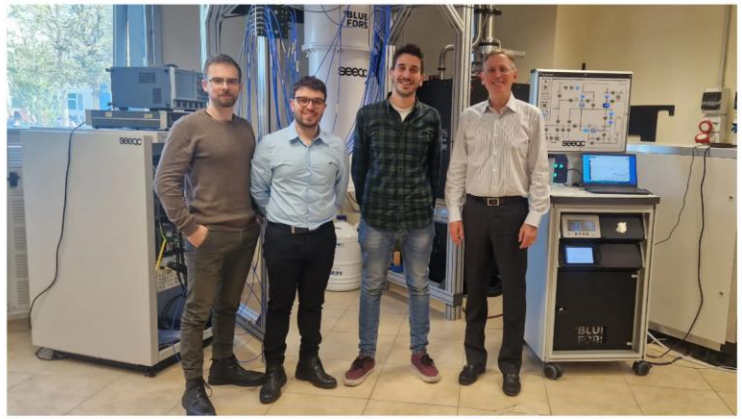
Fully integrated quantum computing architecture

- >8-16x Higher multiplexing, removes overhead
- Built-in error correction
- 1,000x Lower energy and heat dissipation
- >10x Faster clock speeds + lower latency
- 128x Lower control pulse complexity
- Superconducting manufacturing commercial-ready
- 400x Cheaper system components

SEEQC quantum computing systems roadmap

	Analogue (2022) 	Hybrid (2023) 	Digital (2024+) 	
	SEEQC Red class systems Reference systems **SEEQC Red** (Q4 2022) • SEEQC quantum chip – 28us coherence	**SEEQC Orange class systems** Chip-based systems **SEEQC Orange:** DC/SFQ + DEMUX (Q4 2023) • Direct digital control 1:4 Digital MUX - <1 RF I/O per qubit	**SEEQC Yellow class systems** QEC ready systems **SEEQC Yellow: DC/SFQ, SFQ flux + Digital Readout** (Q4 2024) • SEEQC Orange specs + SFQ Z control + JDPD qubit readout, 10ns SFQ logic: 100x lower latency • New Scalable Functionality = Digital readout **SEEQC Bumblebee:** Full SFQ DQM + Reset (TBC) • SEEQC Pumpkin specs + JDPD readout + reset • New feature: Ultra-low latency qubit reset – enables Error correction	**SEEQC Green class systems** Logical systems **SEEQC Green:** Full SFQ DQM + SFQ Decoder (TBC)
Energy Efficiency / Heat dissipation		1000x lower heat dissipation		
Speed & Latency			10x faster readout 10x lower latency	Ultra-low latency cryogenic decoding
Multiplexing		Towards 8x higher multiplexing		
Computational complexity		128x lower control complexity		
Manufacturability			All chip-based system with highly reduced complexity	
Cost			400x cheaper	

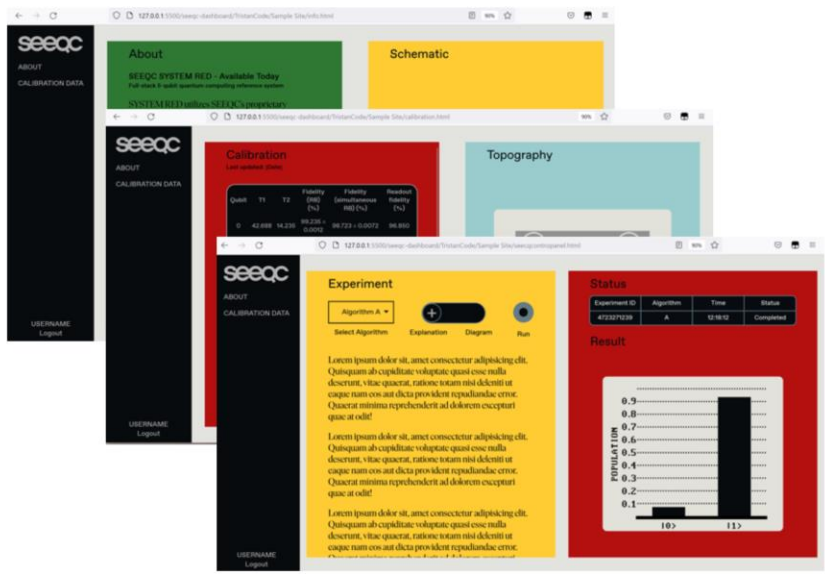
SEEQC Red: first quantum computer in Italy

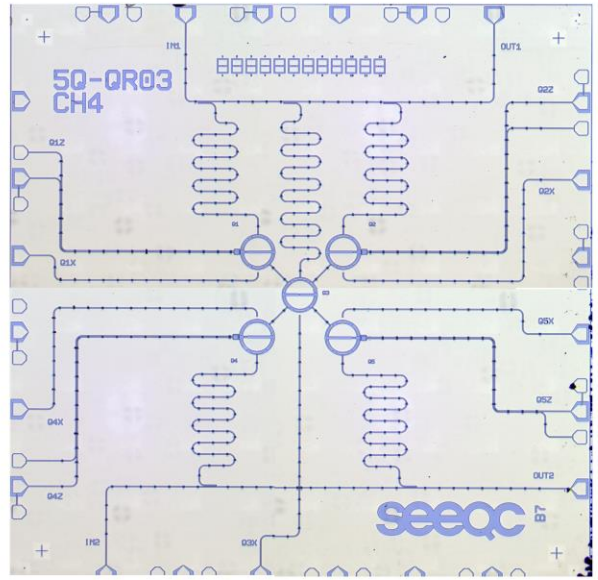


Il team italiano di Seeqc con l'ad John Levy FOTO SANDRO IANNACCONE

SANDRO IANNACCONE SCIENZA 29.04.2023

Abbiamo visto (e provato) il primo computer quantistico in Italia



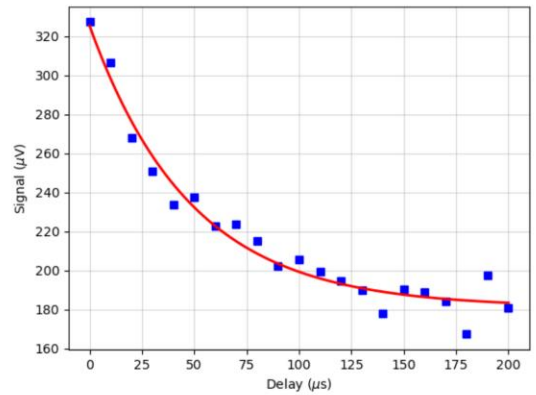


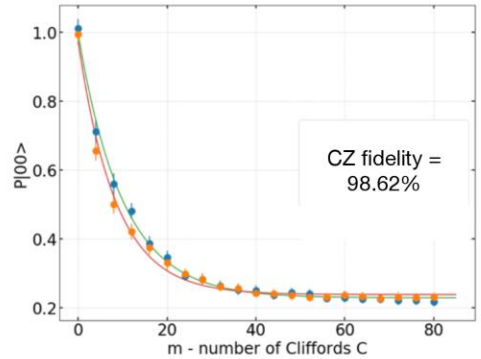
CORRIERE DELLA SERA

Innovazione

L'INDUSTRIA DEL FUTURO

QUANTUM COMPUTER
«PER I CALCOLI ULTRAVELOCI ABBIAMO SCELTO L'ITALIA»





QC + HPC integration:
unifying two communities to solve practical problems

- QPU calibration
- Error mitigation
- Error correction
- Hybrid algorithms

Demand for fast and high-fidelity readout

1. A **scalable** physical system with well characterized qubits
2. The ability to initialize the state of the qubits to a simple fiducial state
3. Long relevant decoherence time
4. A “universal” set of quantum gates
5. A qubit-specific **measurement** capability

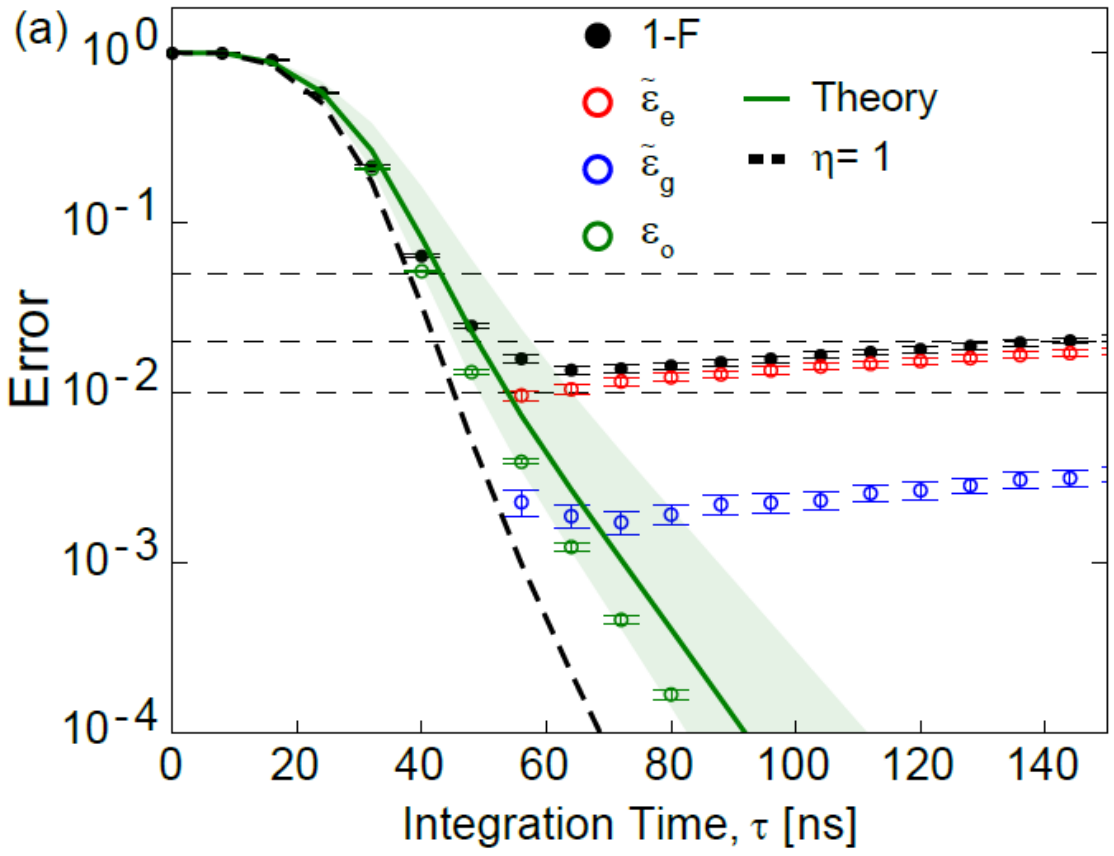
Error thresholds for fault tolerant QC:

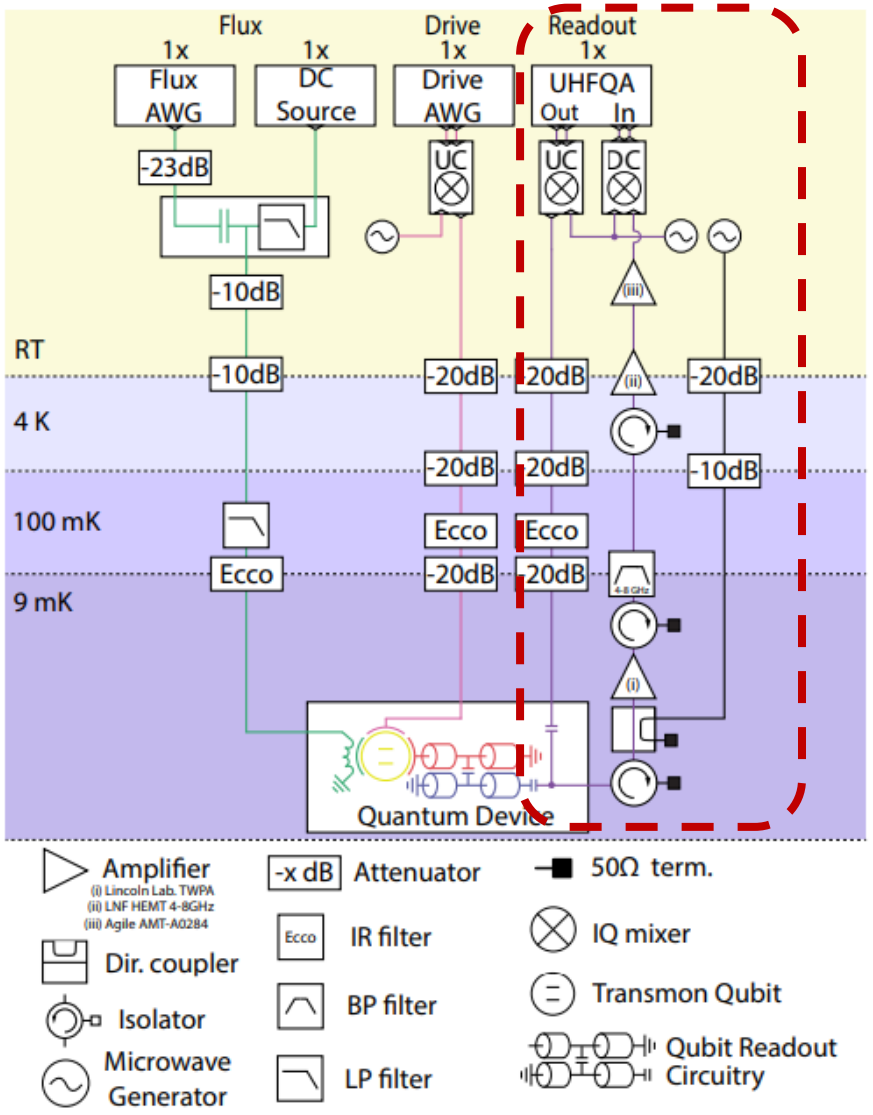
$$\varepsilon_1 \leq 0.1\%$$
$$\varepsilon_2 \leq 0.1\%$$
$$\varepsilon_m \leq 0.5\%$$

D. P. Divincenzo - https://arxiv.org/pdf/quant-ph/0002077.pdf

Martinis, J. M. Qubit metrology for building a fault-tolerant quantum computer. npj Quantum Inform. 1, 15005 (2015).

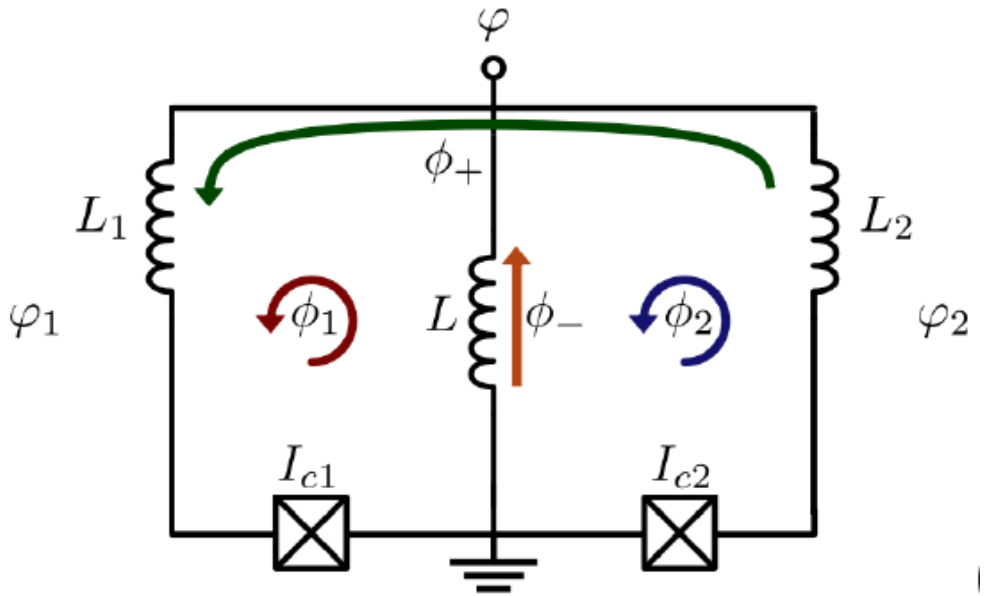
Demand for fast and high-fidelity readout





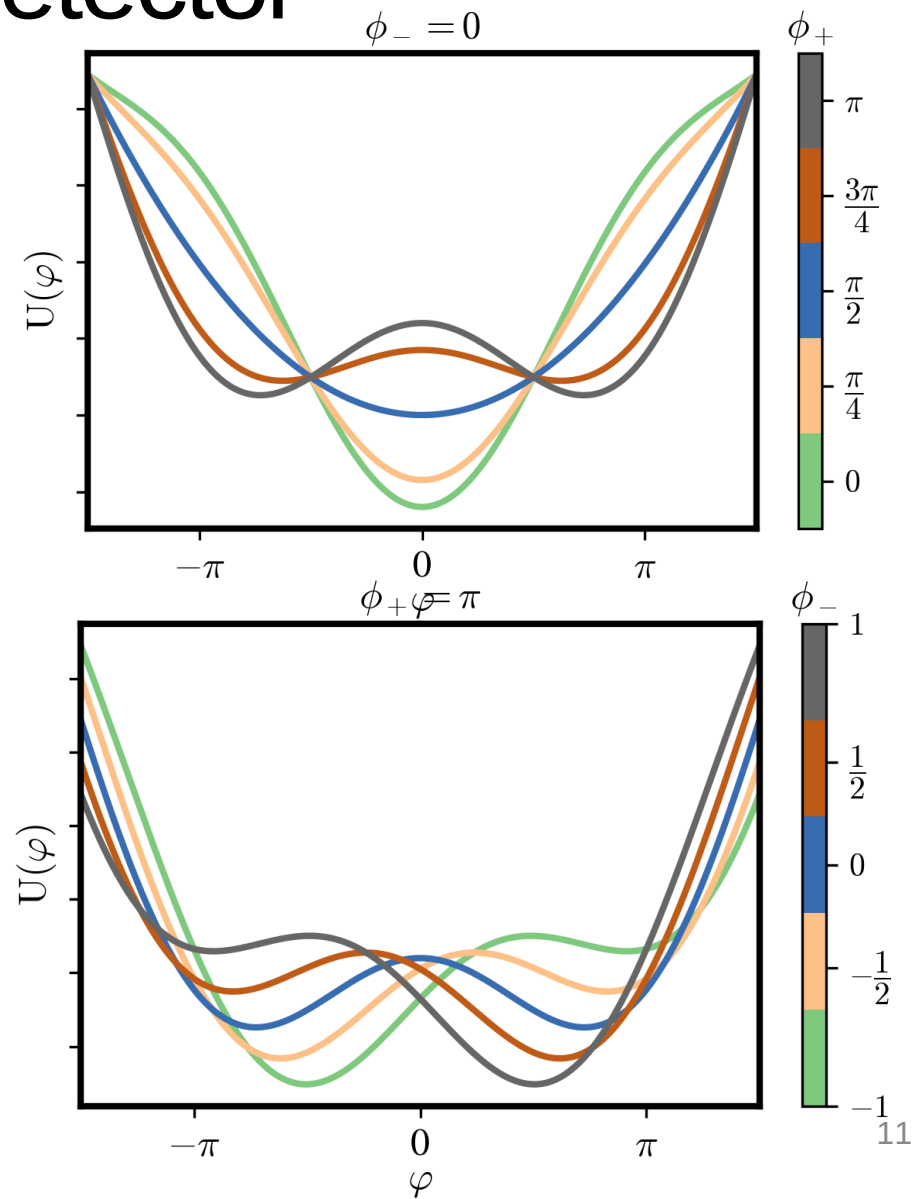
T. Walter, at al., arXiv:1701.06933v2 (2017)
J. Heinsoo, et al. arXiv:1801.07904v1 (2018)
F Swiadek, et al., arXiv:2307.07765 (2023)
L. Chen, at al., npj Quantum Information (2023)

The Josephson Digital Phase Detector



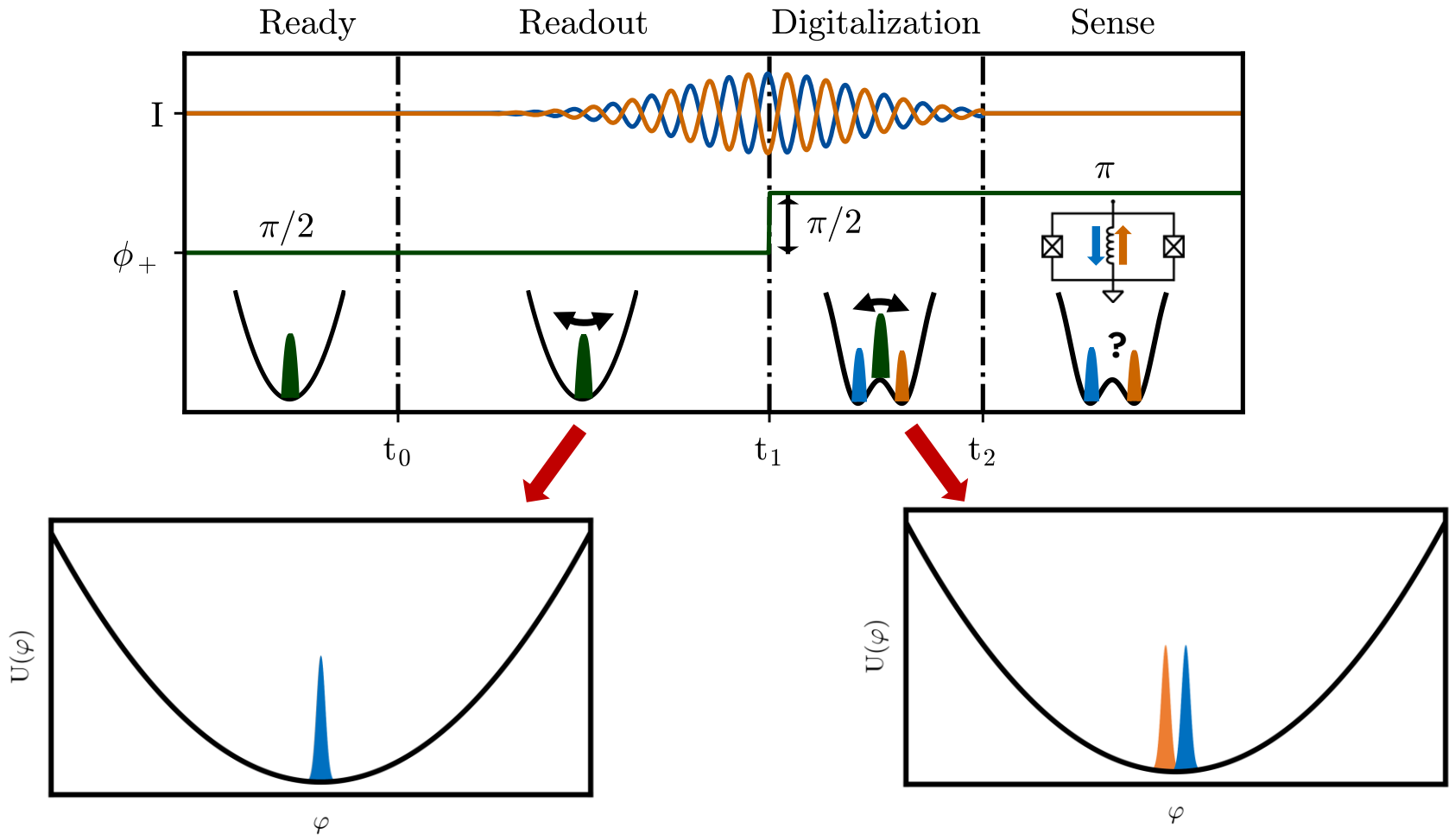
The potential energy can be written as:

$$U(\varphi) = \frac{1}{2L}\left(\frac{\Phi_0}{2\pi}\right)^2 \varphi^2 - \frac{\Phi_0}{2\pi} 2I_c \cos(\phi_- + \varphi)\cos(\phi_+)$$



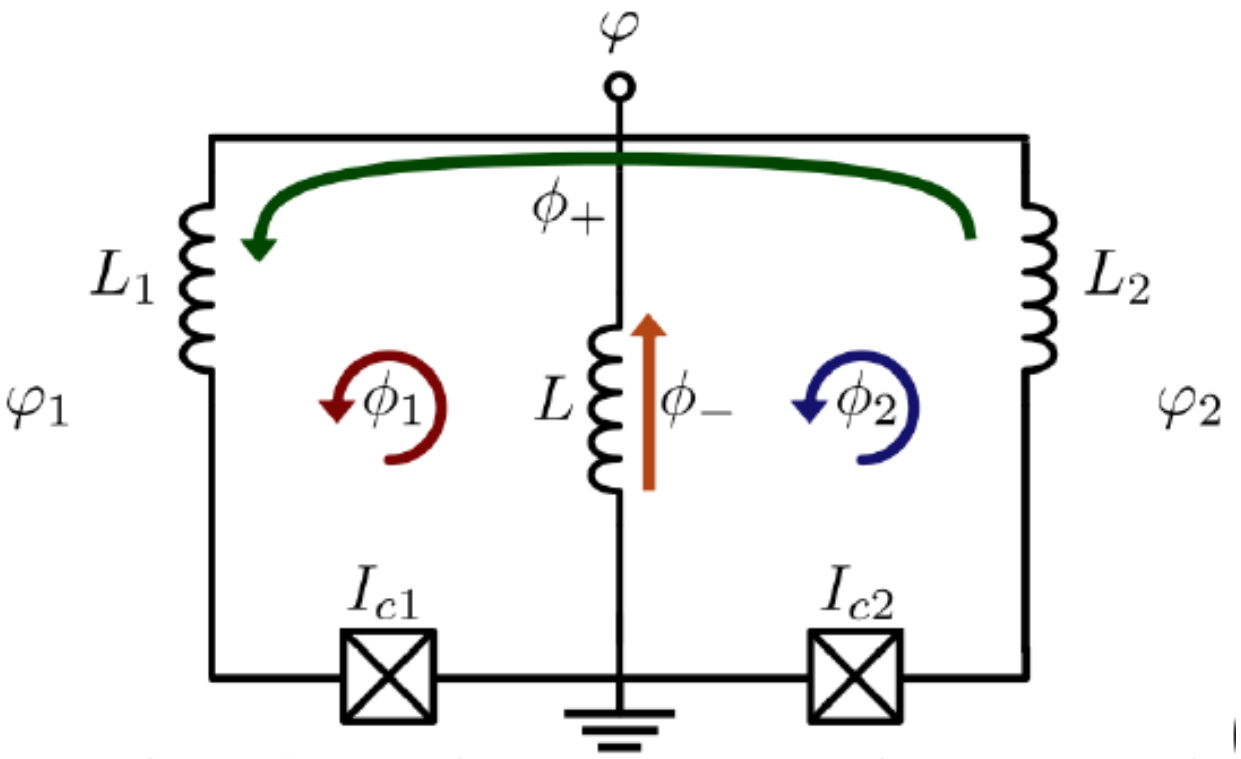
L. Di Palma, et al. Phys. Rev. Applied **19**, 064025 (2023)

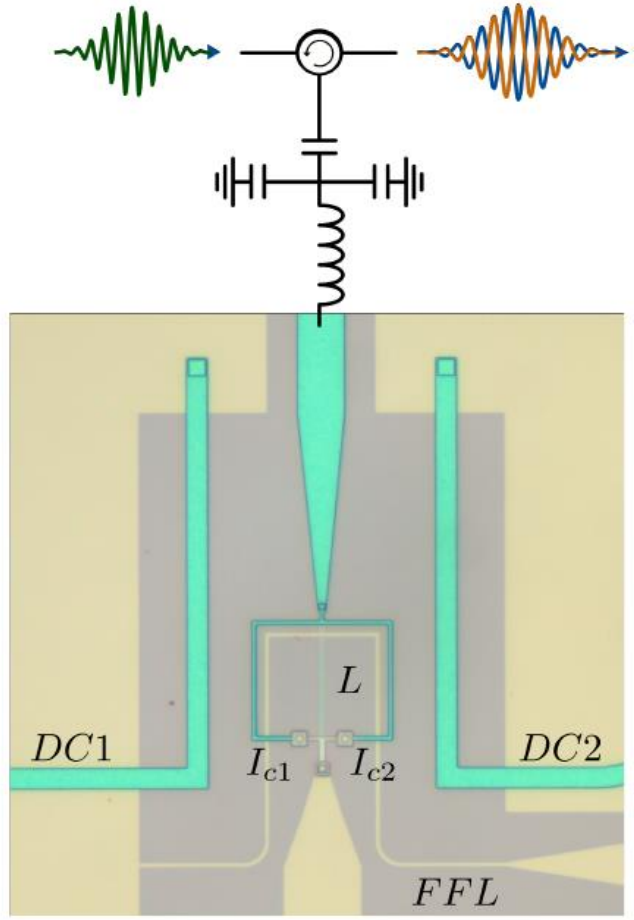
The Josephson Digital Phase Detector



L. Di Palma, et al. Phys. Rev. Applied **19**, 064025 (2023)

Fabrication possible at SEEQC commercial foundry





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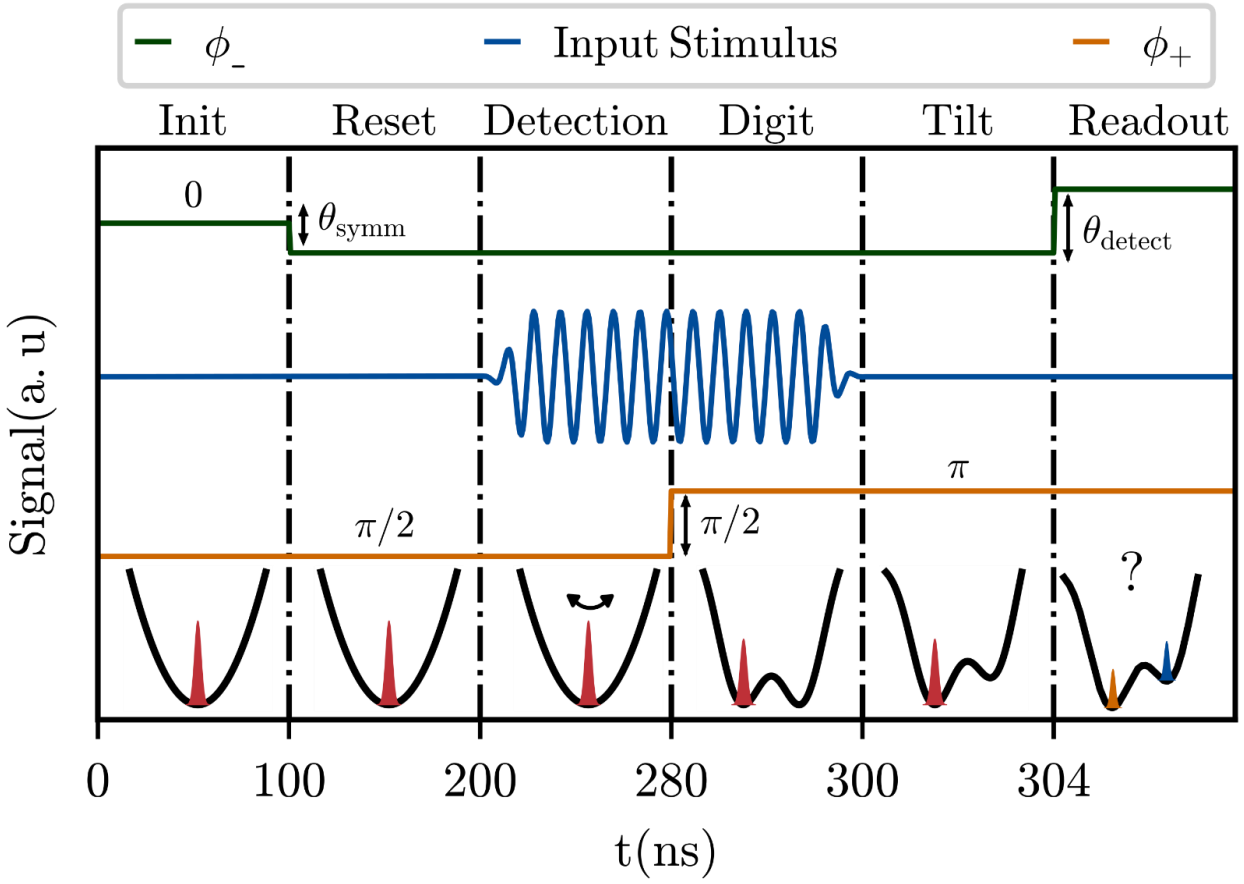
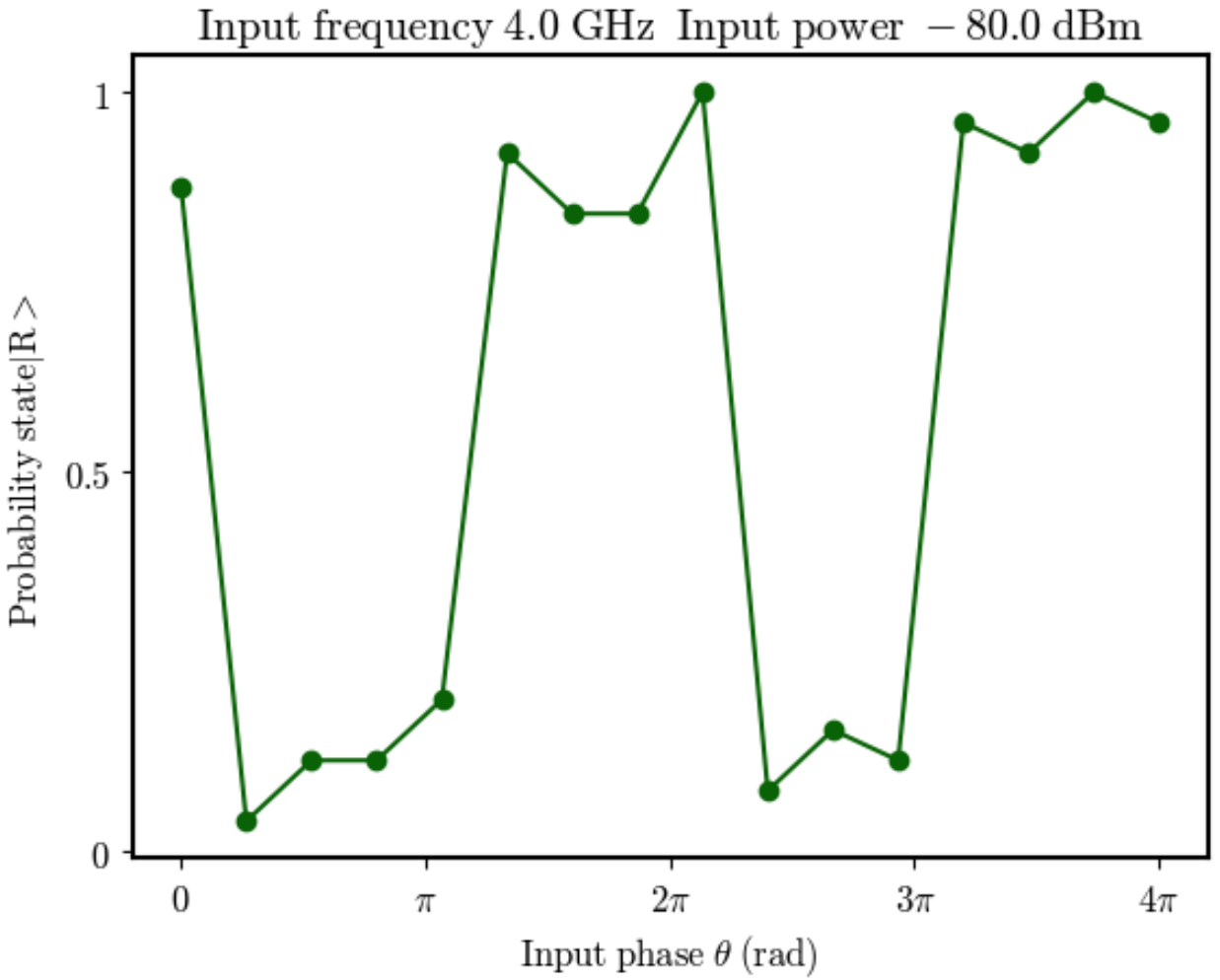
The Josephson Digital Phase Detector



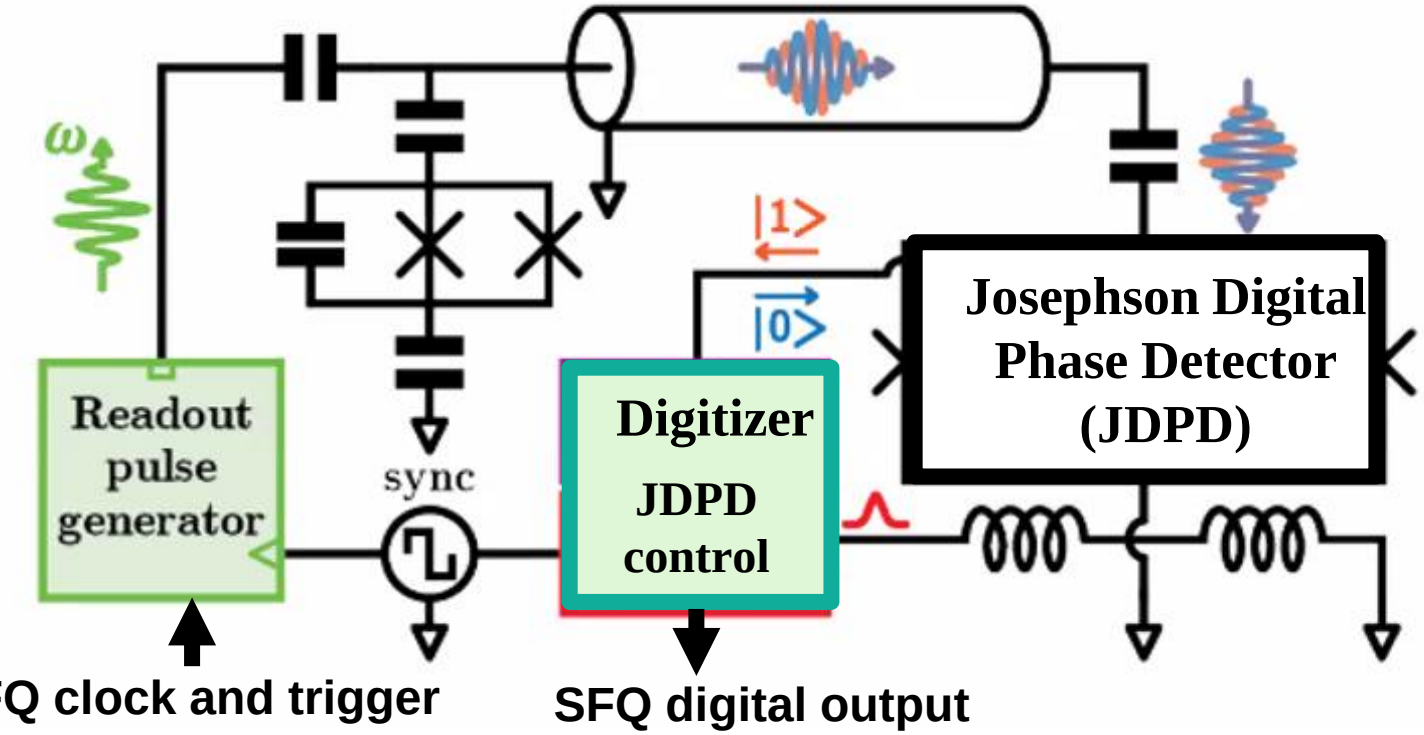


L. Di Palma, et al. Phys. Rev. Applied **19**, 064025 (2023)

The big advantage in scalability comes with SFQ

Quantum-to-Digital Converter:

- Performs phase detection in time domain using co-located superconducting integrated circuit
- Converts output to digital SFQ data
- Readout multiplexing:
  - Digital, e.g., 16:1
  - FDM/TDM 8x1



- Self-contained, co-located readout circuit:
  - ✓ All readout circuits of part of DQM chip MCM-integrated with qubit chip at 20mK
  - ✓ All control signals are generated locally in DQM chip: SFQ master clock and trigger, no external signals

Patent pending

The big advantage in scalability comes with SFQ

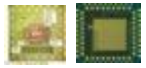
	Conventional readout w JPA/TWPA	JDPD w/o SFQ circuitry	JDPD w SFQ circuitry
Cryo coax lines	3	3	0-1[c]
AWG channels	1-2[a]	3	0
CW RF source	1-2[b]	1	0-1[c]
Digitizer channels	2	2	0
DC/digital lines	0	0	2-5[d]

a. Depending if IQ-mixing or direct digital synthesis of GHz tones is used.
b. The second is needed if IQ-mixing is used for up/down-conversion of GHz tone.
c. Depending if clock is provided from room temperature or generated on-chip.
d. Depending on SFQ-circuits design.

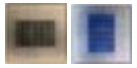
SFQ-based on chip digital readout

SEEQC solution:
Multi-layer Processors in Dilution Refrigerator

High-speed digital SFQ co-processors +
cryoCMOS memory and co-processors



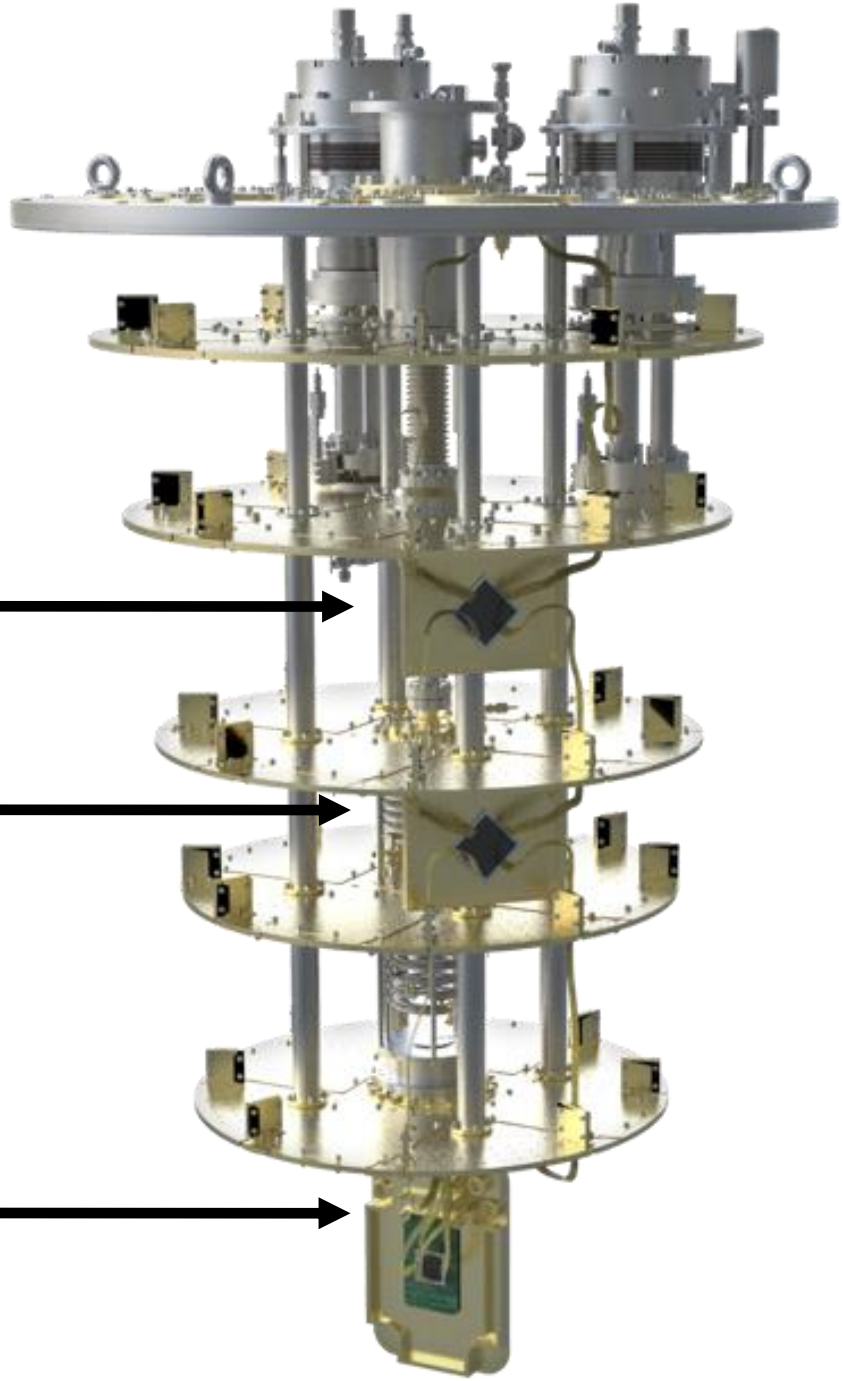
High-speed digital SFQ controller
+ QEC pre-decoder



Multi-Chip Module (MCM)

Quantum Layer

Fit onto a multi-chip module on top
of qubits in DR



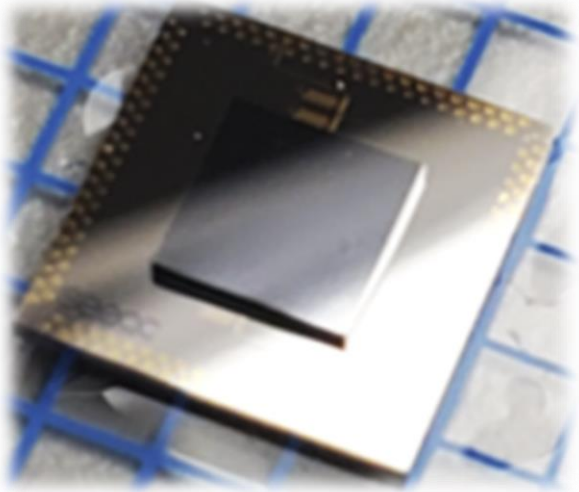
Working towards a data link from QC to HPC

SEEQC Announces Digital Chip-Based Collaboration with NVIDIA to Accelerate Quantum Supercomputing

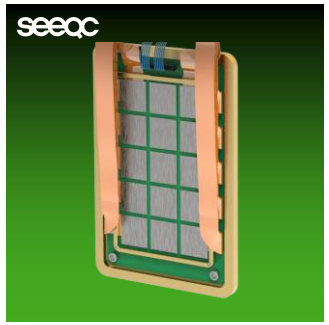
World's first fully digital chip-based quantum-to-GPU integration will enable error-corrected quantum supercomputing

Why it matters…

- The successful integration of SEEQC's chip architecture with NVIDIA GPUs will:
  - Create a chip-based quantum-to-GPU computing solution, compatible with all quantum computing technologies (superconducting, silicon spin, photonics, trapped ion, neutral and cold atom, topological).
  - Combine the best of classical and quantum computing into Quantum Supercomputing.
  - Bring quantum computing closer to datacenter-scale with infrastructure for quantum AI.
  - Create the possibility for on-chip, real-time quantum error correction that is necessary for qu computers to scale.



SEEQC Single Flux Quantum (SFQ) microprocessor chip



SEEQC Orange/Yellow/Green systems + SEEQC Control core platform

Quantum enhanced data center


seeqc
Thank you