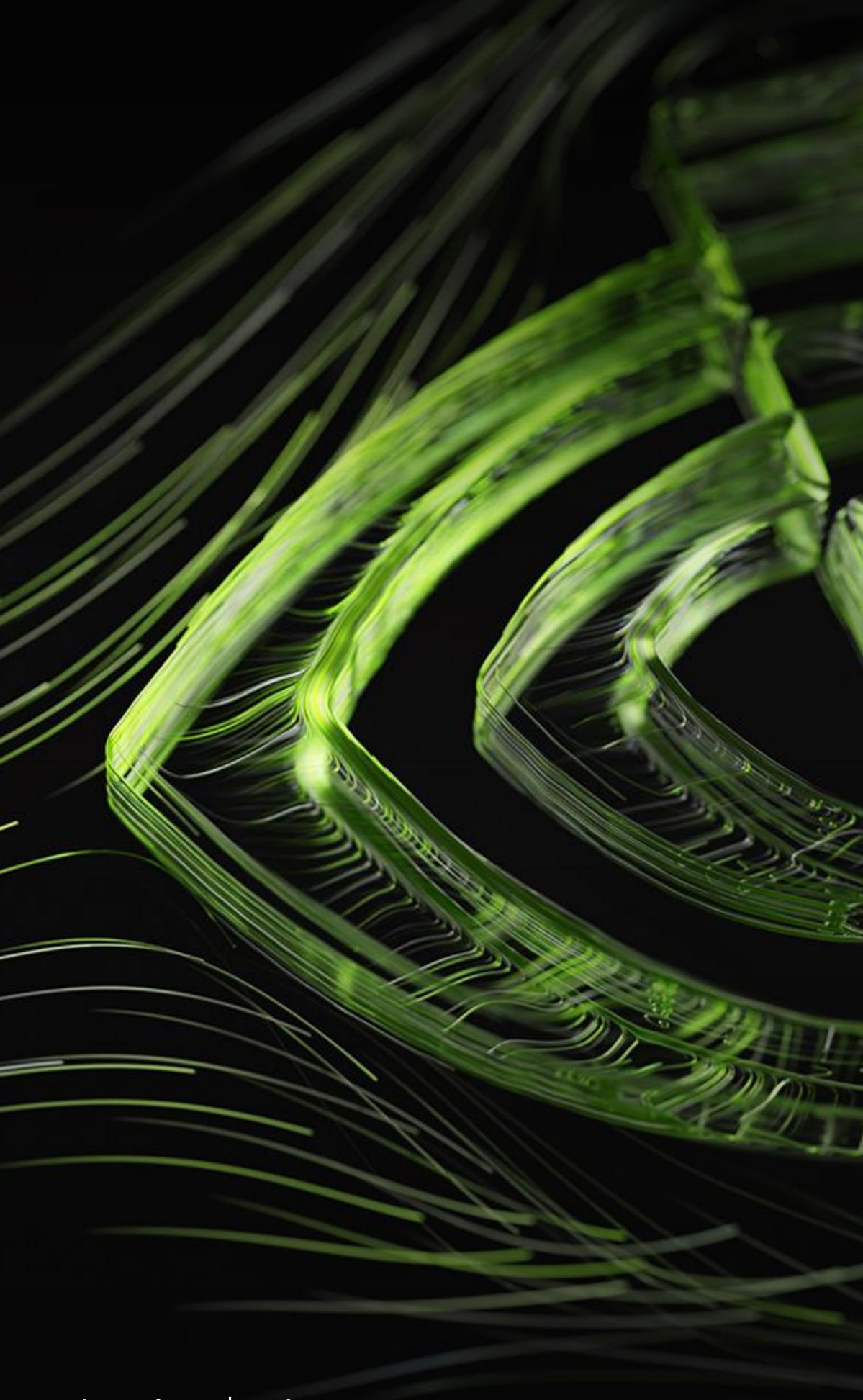


NVIDIA Day CINECA Practical Quantum Computing School 2nd Edition



Dec 2nd 2022





Agenda

- Introduction
- NVIDIA cuQua
- NVIDIA cuQua cuTensorNet
- **NVIDIA QODA**
- Qibo and cuQu
- Hands-on exercises with Qibo

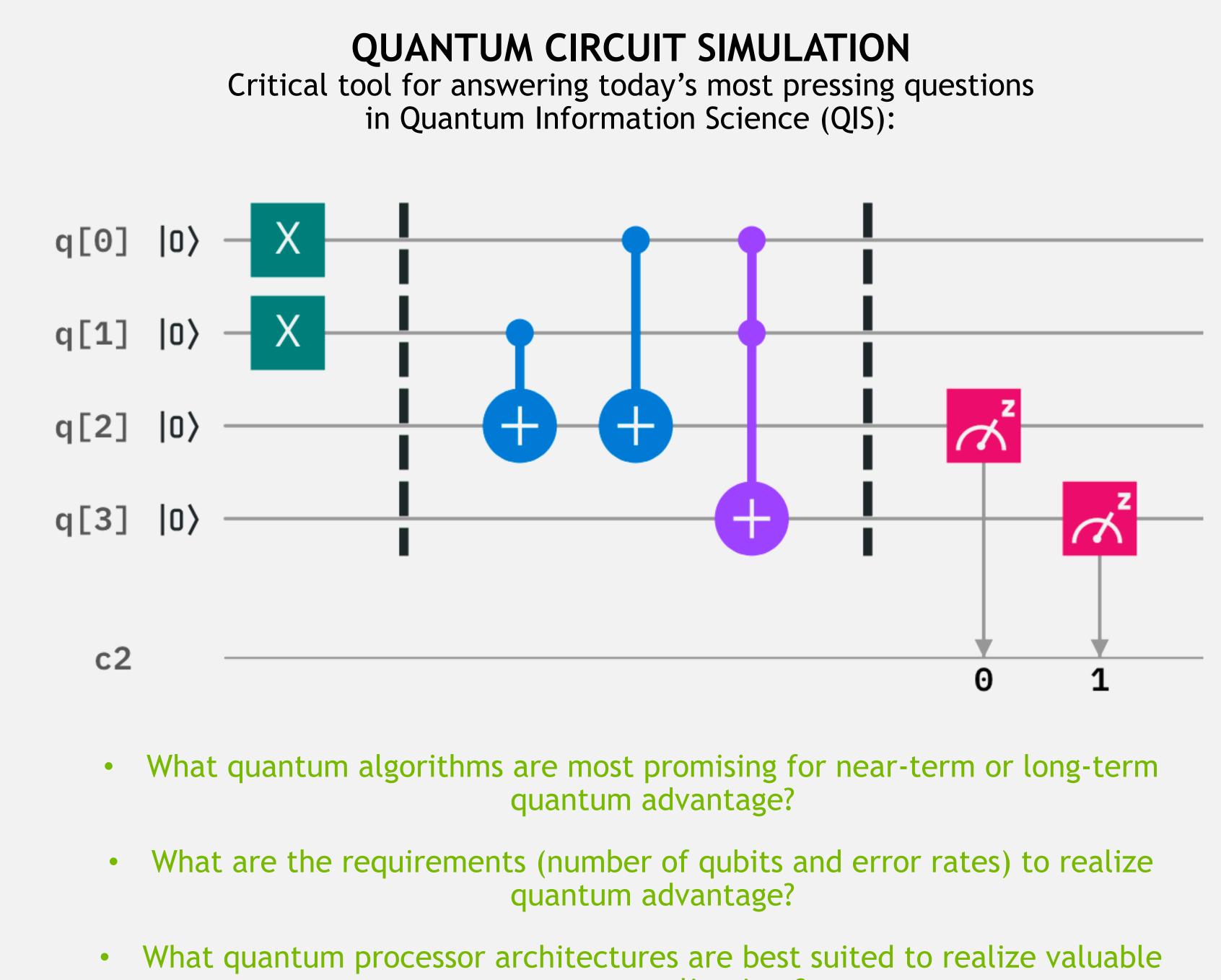


antum	Carlo Nardone, NVIDIA	
antum:	Andreas Hehn, NVIDIA	
٩	Zohim Chandani, NVIDIA	
Quantum integration	Andrea Pasquale, UniMI Stavros Efthymiou, TII	
ercises with Qibo		

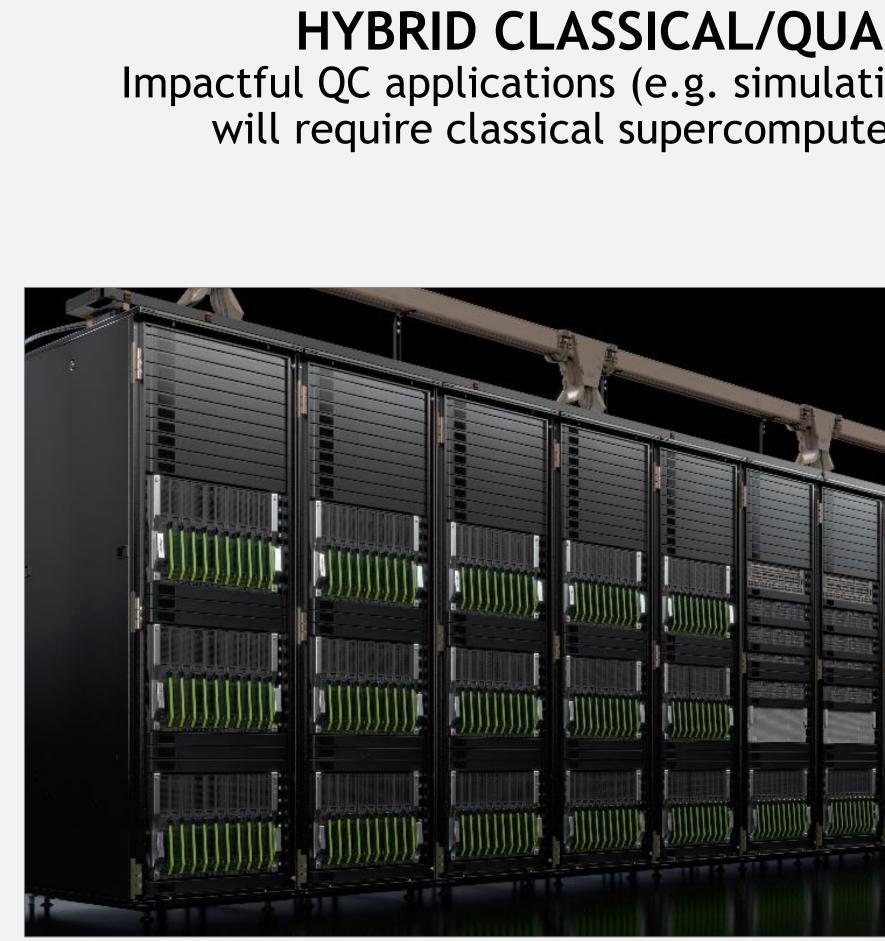
Quantum Computing Simulation



GPU-based Supercomputing in the Quantum Computing Ecosystem Researching the quantum computer of tomorrow with the supercomputers of today



- quantum applications?



- •
- How can we allow domain scientists to easily test coprogramming of QPUs with classical HPC systems?

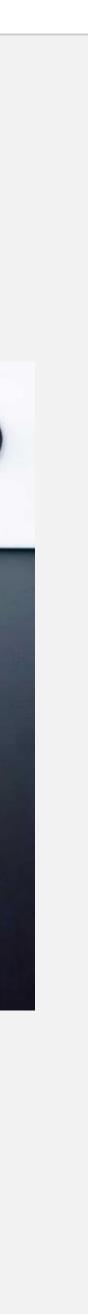
HYBRID CLASSICAL/QUANTUM APPLICATIONS

Impactful QC applications (e.g. simulating quantum materials and systems) will require classical supercomputers with quantum co-processors



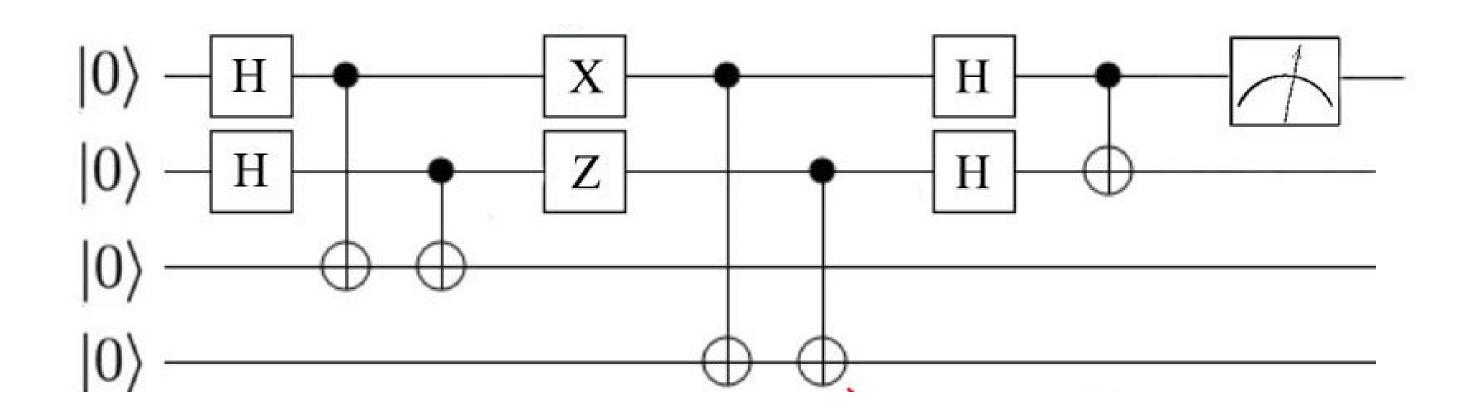
How can we integrate and take advantage of classical HPC to accelerate hybrid classical/quantum workloads?

• Can we take advantage of GPU acceleration for circuit synthesis, classical optimization, and error correction decoding?





Two Leading Quantum Circuit Simulation Approaches



State vector simulation

"Gate-based emulation of a quantum

- Maintain full 2ⁿ qubit vector state i
- Update all states every timestep, p of the states for measurement

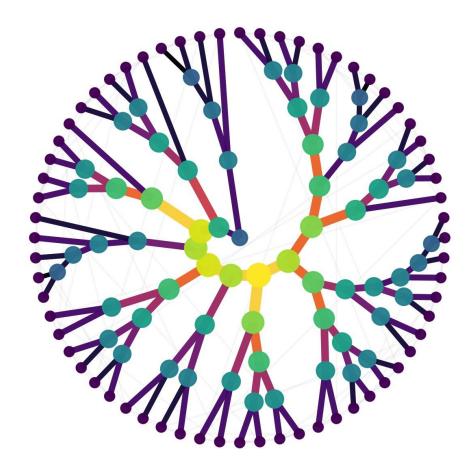
Memory capacity & time grow exponentially w/ # of practical limit around 50 qubits on a supercomputer

Can model either ideal or noisy qubits

n computer"	"Only sim	
in memory	• Uses t	
probabilistically sample n	reduceCan si	
ntially w/ # of qubits -	practi	

GPUs are a great fit for either approach

Source of Tensor Network image: Quimb - quimb.readthedocs.io



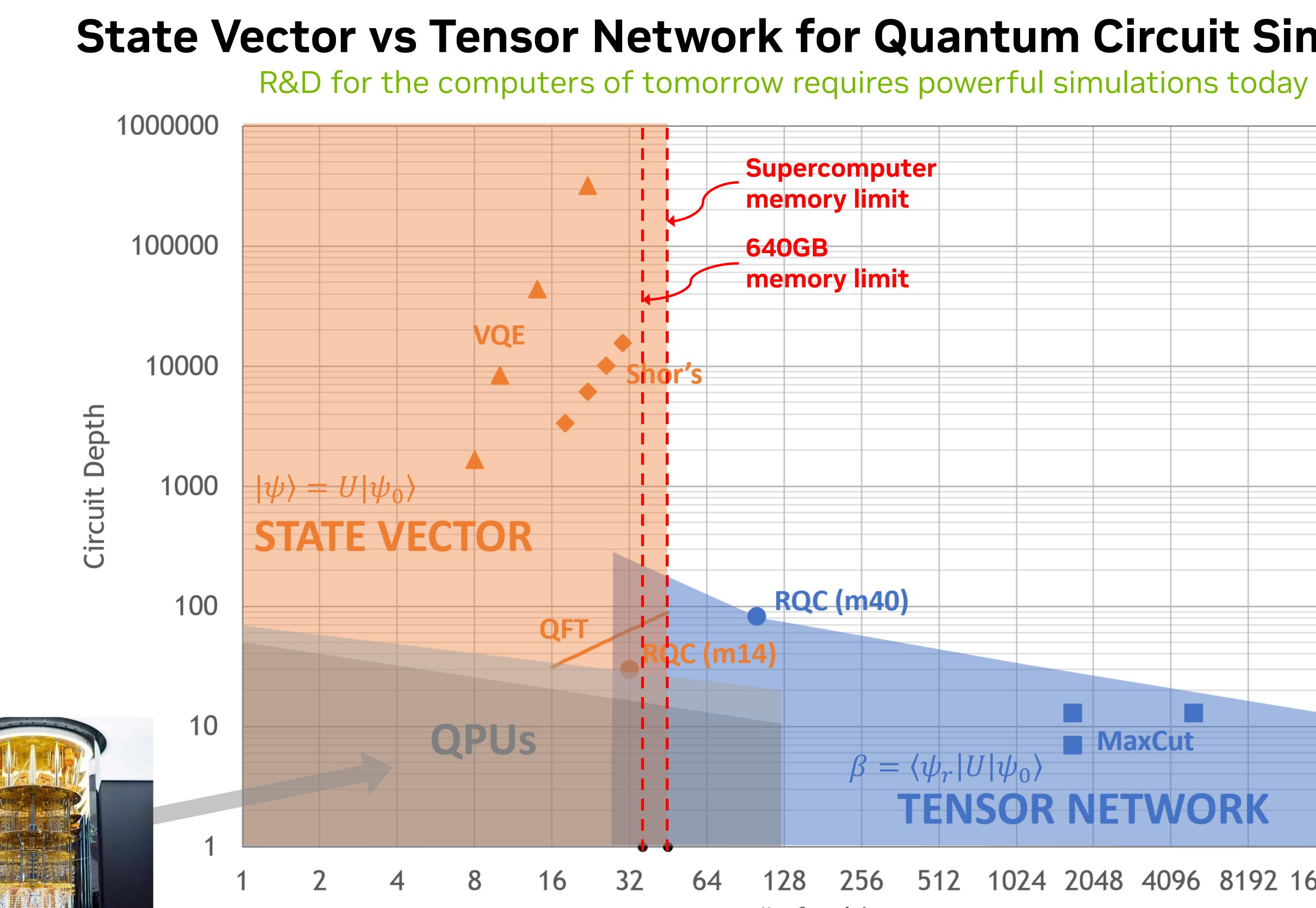
Tensor networks

nulate the states you need"

tensor network contractions to dramatically certain tensor network contractions to dramatically certains

imulate 100s or 1000s of qubits for many ical quantum circuits







State Vector vs Tensor Network for Quantum Circuit Simulation

of qubits

_		 	
1			
]			
1			
1			
-			
_		 	
1			
_		 	
-		 	
_			
1			
_		 	
_		 	
- 1	-		
	L		
	$ _0\rangle$ —		
	$ _0\rangle$ —		
	$ _0\rangle$ —		

512 1024 2048 4096 8192 16384 32768



NVIDIA cuQuantum



cuQuantum is an SDK of optimized libraries and tools for accelerating Quantum Computing workflows

- cuQuantum is **not** a:
 - Quantum Computer
 - Quantum Computing Framework
 - Quantum Circuit Simulator
- Very similar approach to what NVIDIA has done in the past in the CUDA ecosystem
 - cuBLAS, cuFFT ...
 - cuDNN invoked by all major Deep Learning frameworks (PyTorch, TensorFlow, etc.)

Introducing cuQuantum



Quantum Computing Application

Quantum Computing Frameworks (eg Cirq, Qiskit)

Quantum Circuit Simulators (eg Qsim, Qiskit-aer)

cuQuantum

cuTensorNet

QPU

GPU Accelerated Computing



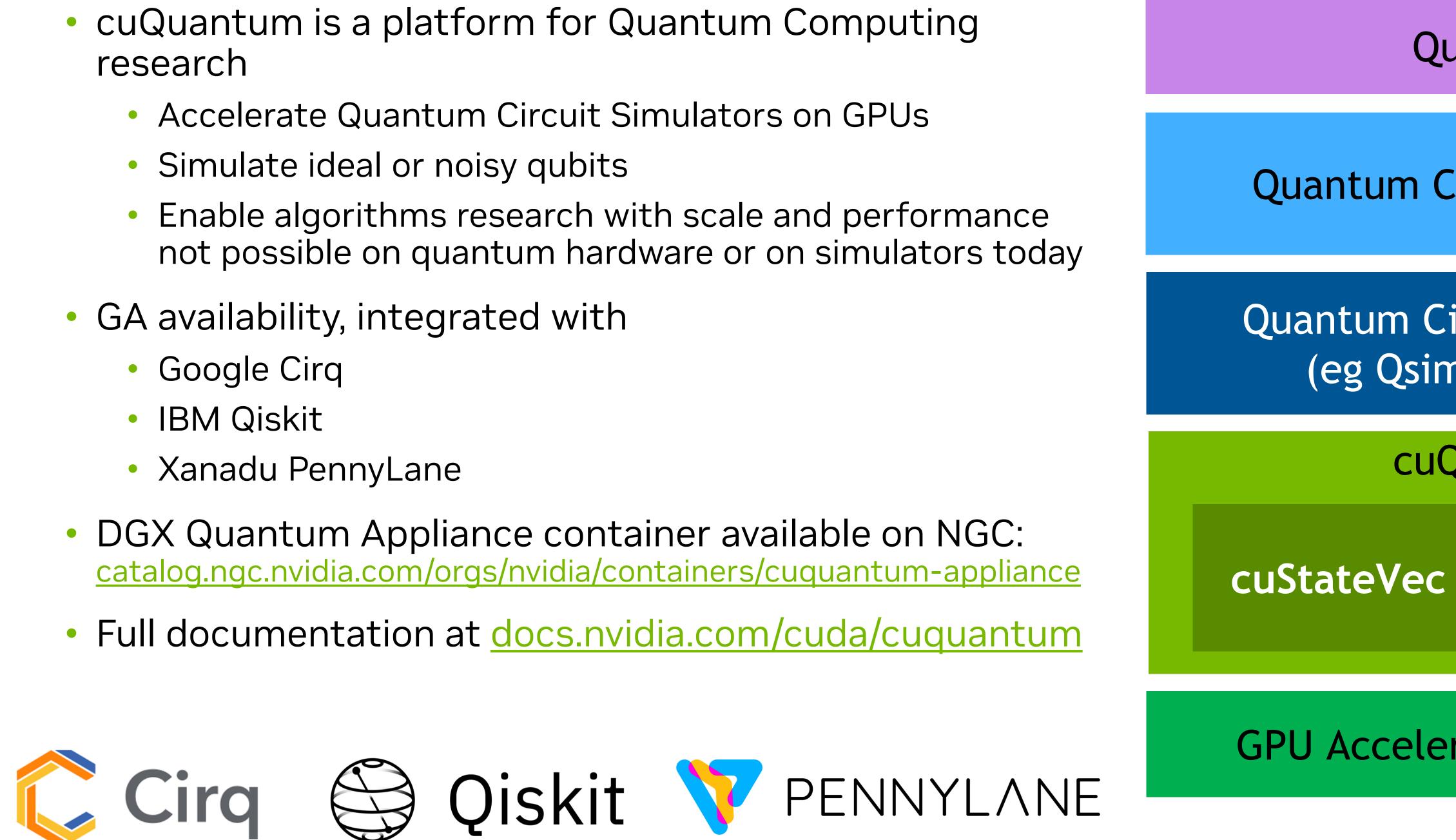


- cuQuantum is a platform for Quantum Computing research
 - Accelerate Quantum Circuit Simulators on GPUs
 - Simulate ideal or noisy qubits
 - Enable algorithms research with scale and performance not possible on quantum hardware or on simulators today
- GA availability, integrated with
 - Google Cirq
 - IBM Qiskit
 - Xanadu PennyLane
- DGX Quantum Appliance container available on NGC: catalog.ngc.nvidia.com/orgs/nvidia/containers/cuquantum-appliance
- Full documentation at <u>docs.nvidia.com/cuda/cuquantum</u>





Introducing cuQuantum



Quantum Computing Application

Quantum Computing Frameworks (eg Cirq, Qiskit)

Quantum Circuit Simulators (eg Qsim, Qiskit-aer)

cuQuantum

cuTensorNet

QPU

GPU Accelerated Computing





Frameworks

















cuQuantum Ecosystem







QUANTINUUM CONQ $X \land N \land D U$ ZAPATA



Other Power Users





Ψ**PsiQuantum**

PASQAL QUANTUM BRILLIANCE **CLASSIQ QCWARE** menten.AI







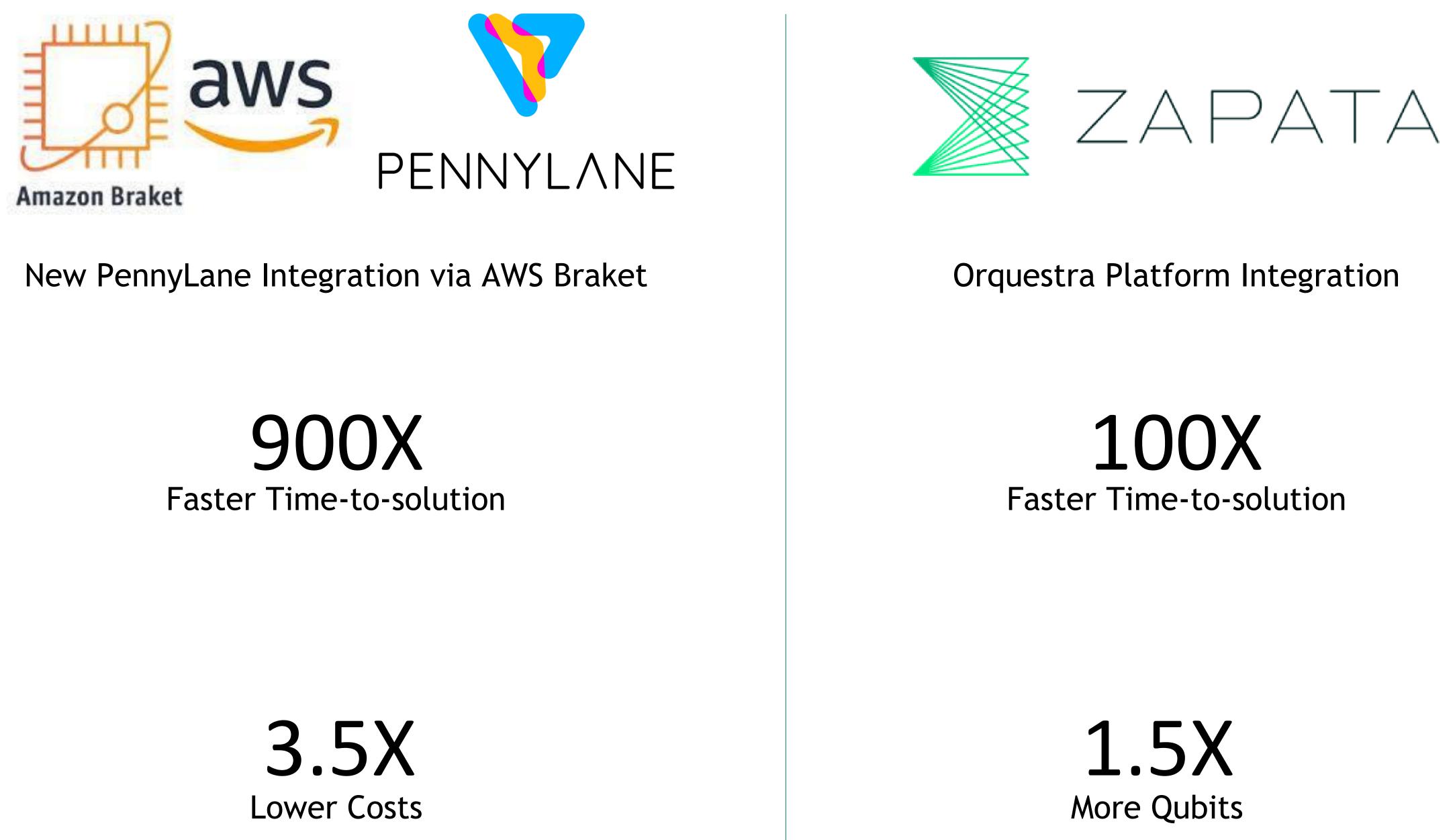
Faster Quantum Algorithm for Physics-ML

Faster Time-to-solution

24X More Circuit Depth

cuQuantum Performance

Enabling speedups for a range of use cases and users



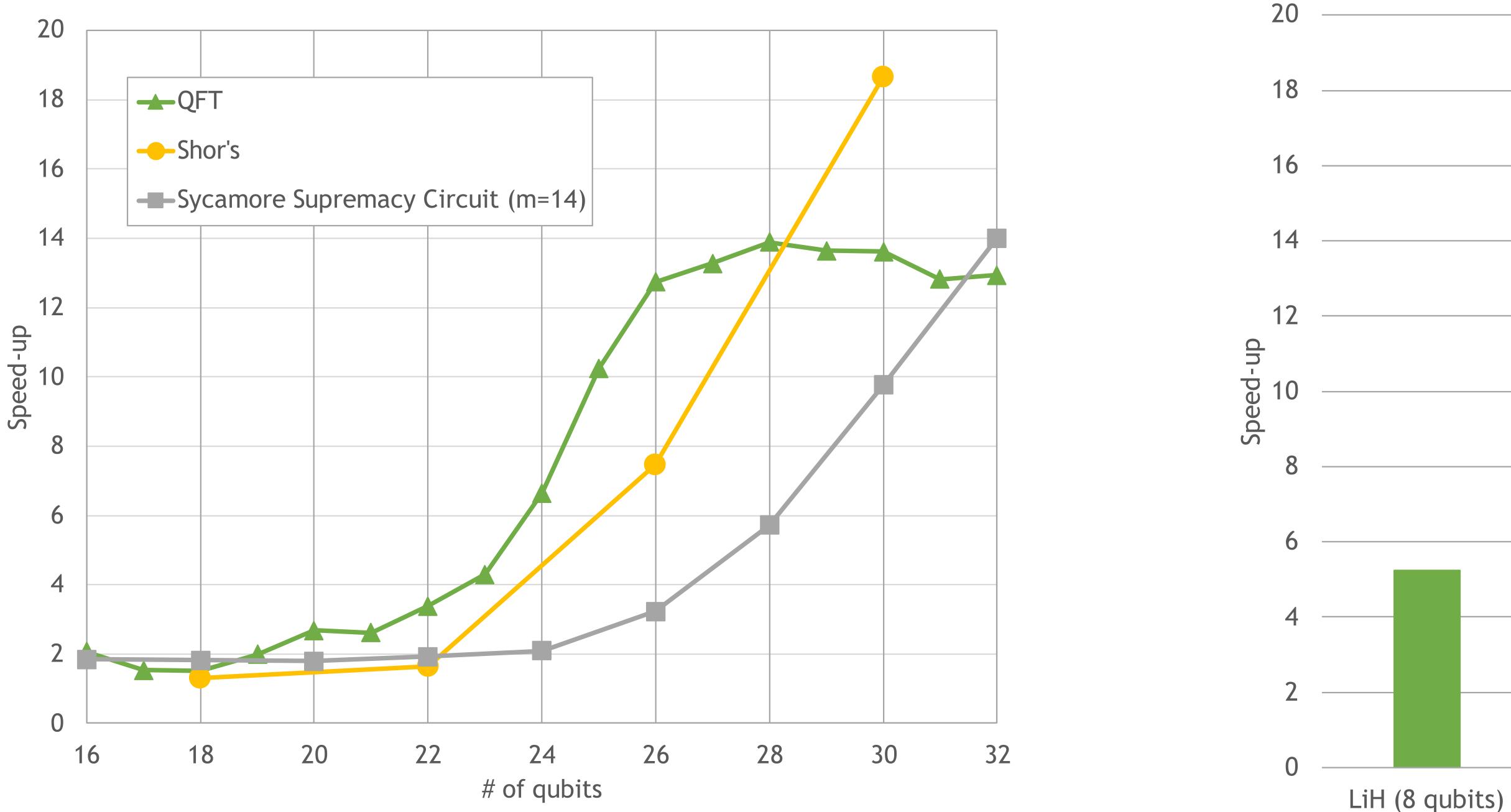






cuStateVec – Single GPU Performance Preliminary performance of Cirq/Qsim + cuStateVec on NVIDIA A100

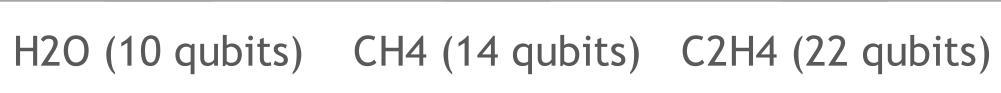
A100 80G vs 64 core CPU



Benchmarks run using cirq/qsim with modifications to integrate cuStateVec CPUs used were AMD EPYC 7742 with 64 cores QFT circuit with 32 qubits and depth 63 Shor's circuit with 30 qubit and depth 15560 (integer factorized: 65) Sycamore supremacy circuit m=14 with 7480 gates VQE benchmarks have all orbitals and results were measured for the energy function evaluation

VQE speed-up relative to single CPU

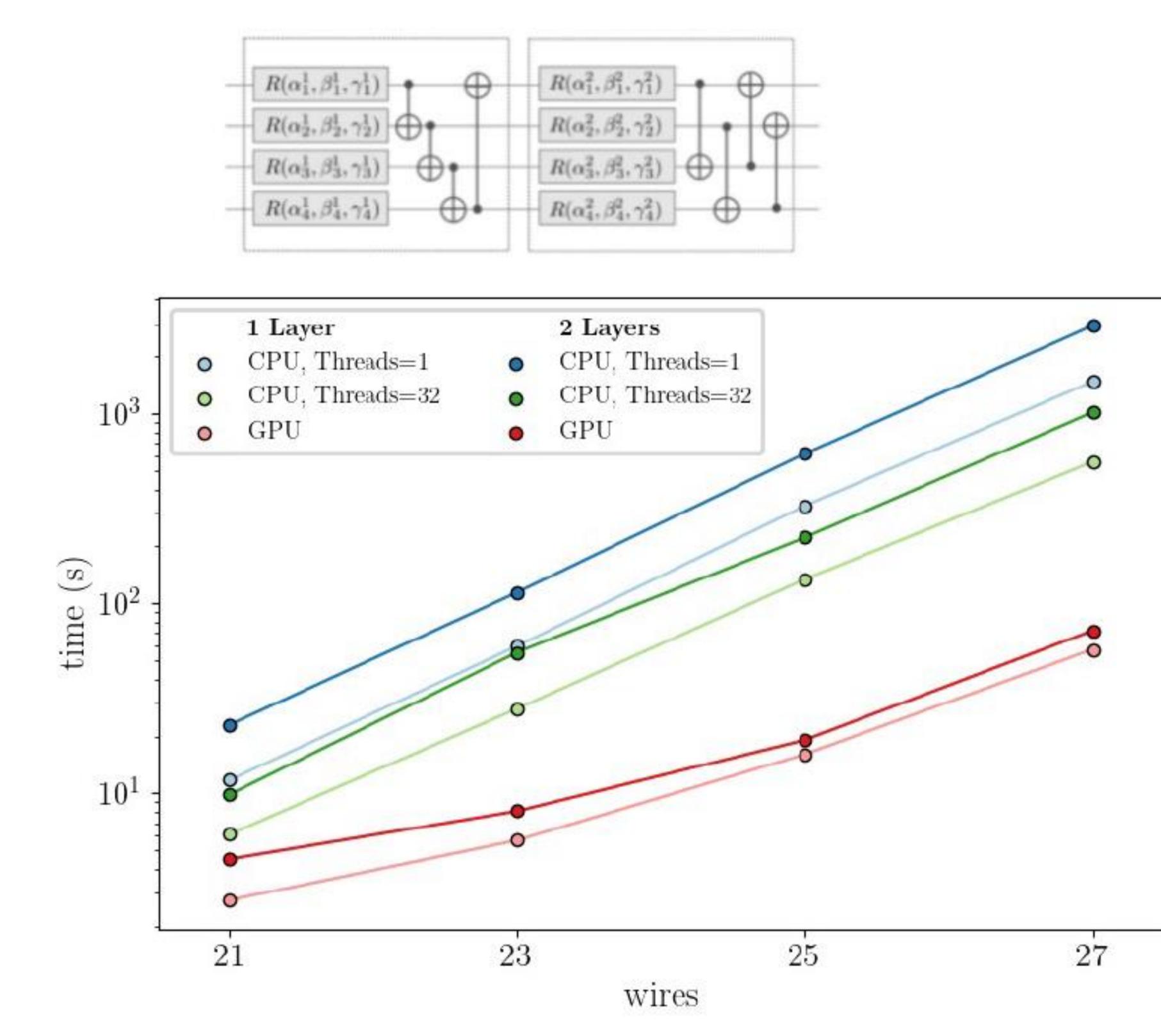
	-	
1 (0, a) = b = b = 120 (40, a) = b = b = 0	(22)	



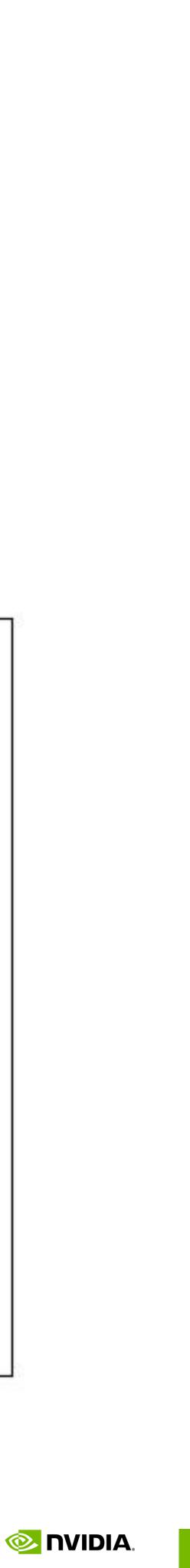
cuQuantum Support for PennyLane

- Leading open-source framework for quantum machine learning and quantum chemistry, built by Xanadu
 - Train Quantum Computers in the same way as Neural Networks
- New simulator *lightning.gpu* with cuQuantum support, available now:
 - <u>xanadu.ai/products/lightning</u>
- 10x speedup for QML circuits





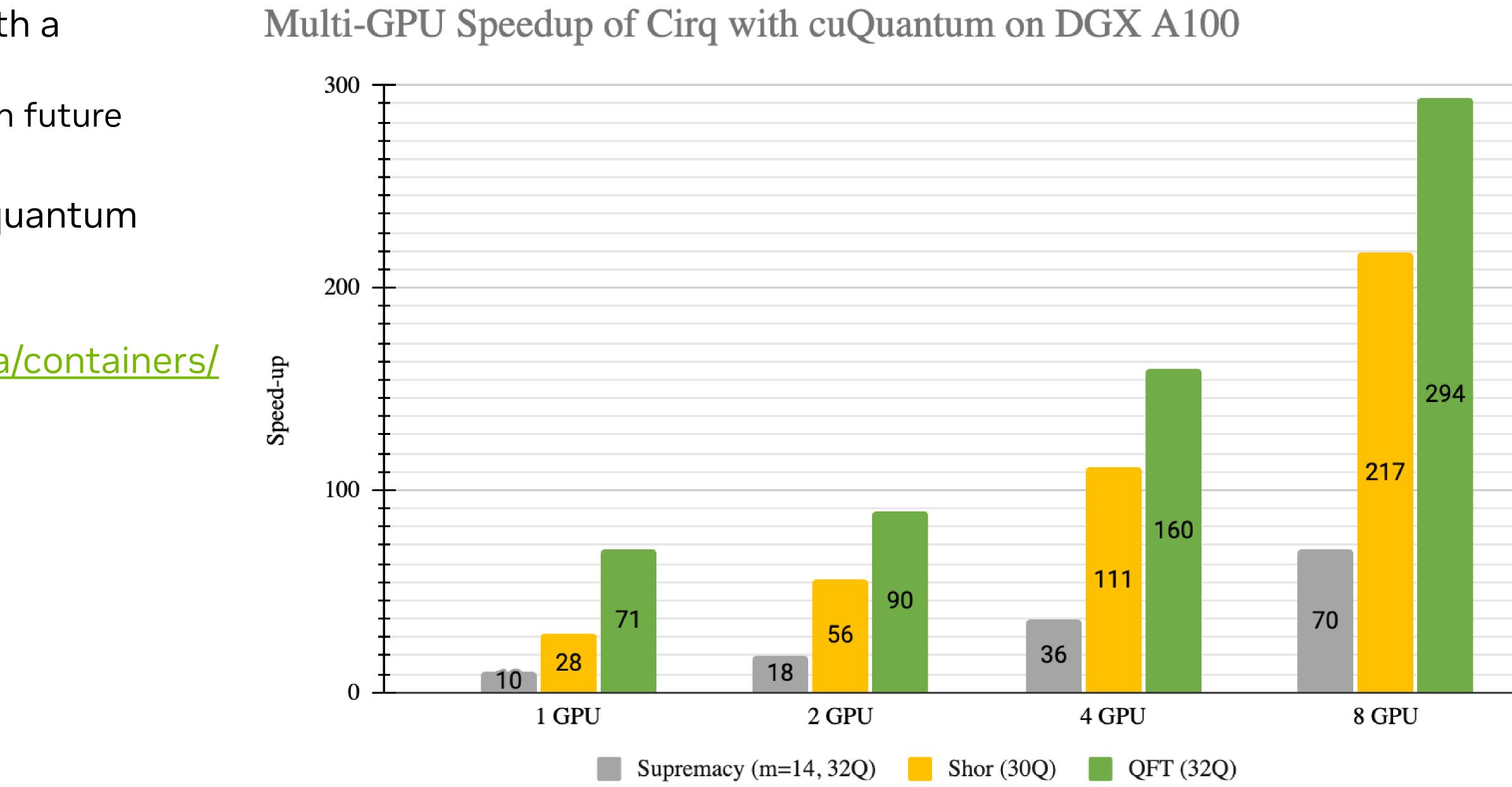




- Full Quantum Simulation stack with a Cirq/Qsim frontend
 - other frontends will be available in future releases
- World class performance on key quantum algorithms, multi-GPU optimized
- Available now on NGC: catalog.ngc.nvidia.com/orgs/nvidia/containers/ <u>cuquantum-appliance</u>



DGX cuQuantum Appliance Multi-GPU container with cuQuantum + integrated Cirq/Qsim







Demo 1: cuQuantum in Cirq



Demo 2: QML with PennyLane





Demo 3: VQE circuit with cuStateVec



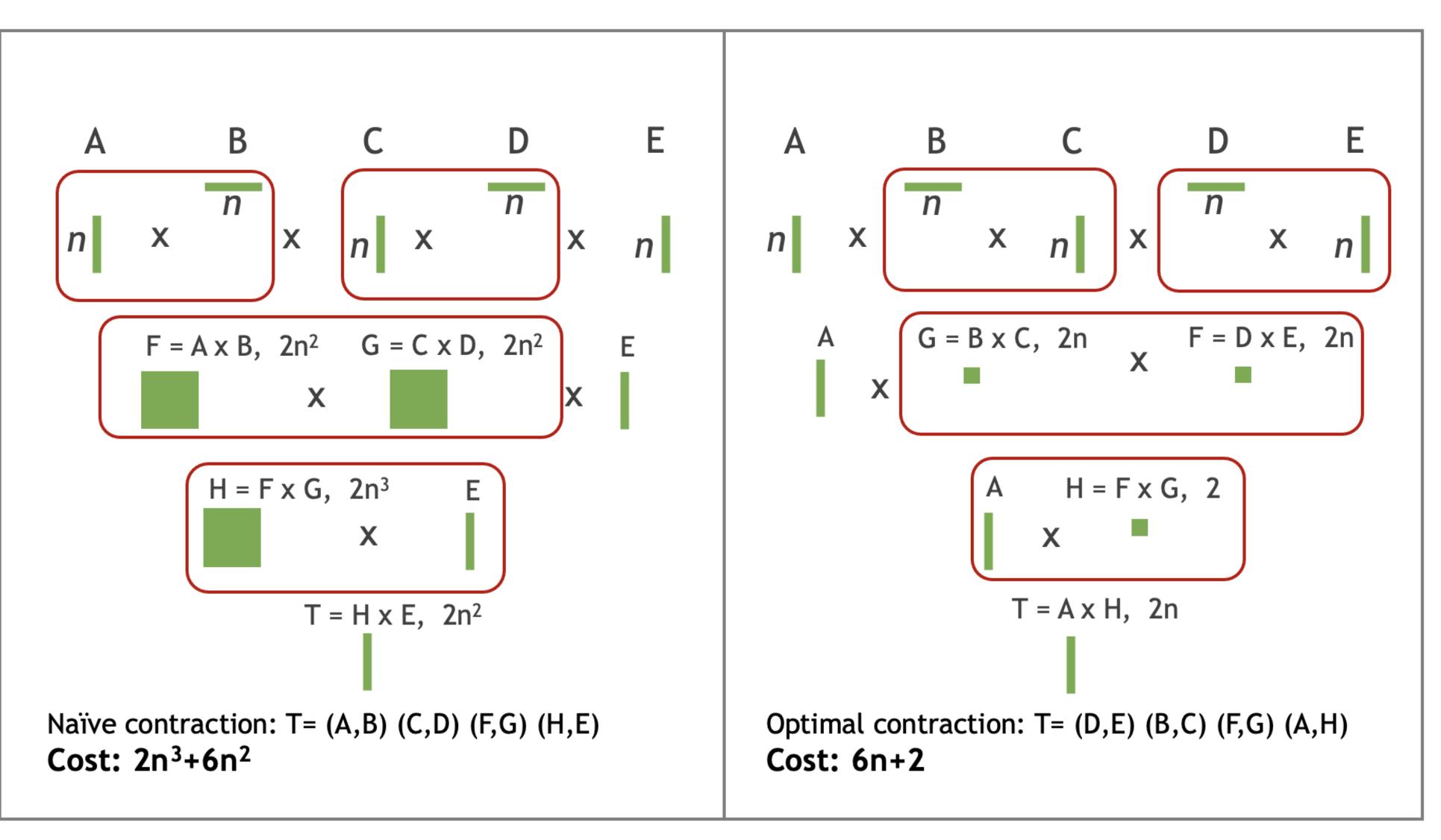
Tensor Networks & MaxCut

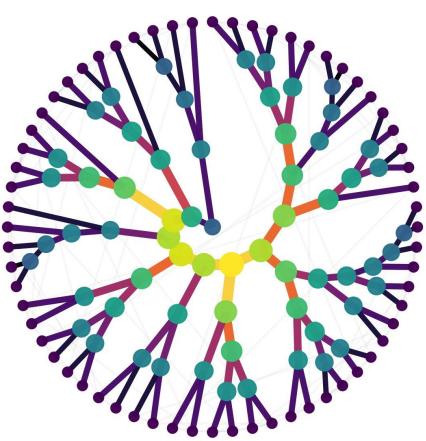


- For many practical quantum circuits, tensor networks enable scaling of simulation to 100s or 1000s of qubits
- cuTensorNet provides APIs to:
 - convert a circuit written in Cirq or Qiskit to a tensor network
 - calculate an optimal path for the contraction
 - hyper-optimization is used to find contraction path with lowest total cost (eg FLOPS or time estimate)
 - slicing is introduced to create parallelism or reduce maximum intermediate tensor sizes
 - calculate an execution plan and execute the TN contraction
 - leverages cuTENSOR heuristics
- Checkout technical blogpost on NVIDIA Devblog: developer.nvidia.com/blog/scaling-quantum-circuitsimulation-with-cutensornet

cuTensorNet

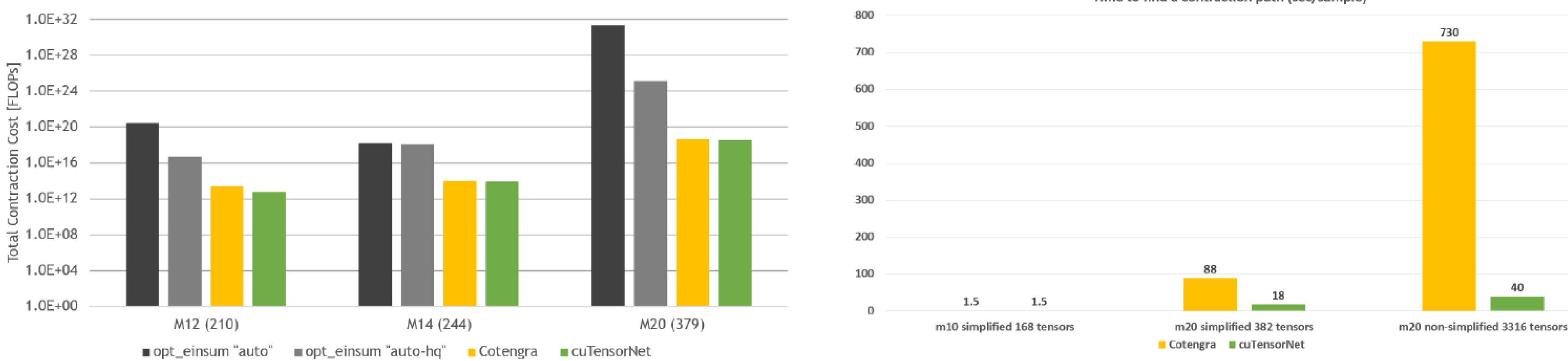
A library to accelerate Tensor Network based Quantum Circuit simulation







Quality of Path



cuTensorNet achieves SotA pathfinding results dramatically faster, and does better with more complex networks

[1] Gray & Kourtis, Hyper-optimized tensor network contraction, 2021. URL: <u>quantum-journal.org/papers/q-2021-03-15-410/pdf</u> [2] opt-einsum, URL: <u>pypi.org/project/opt-einsum</u>

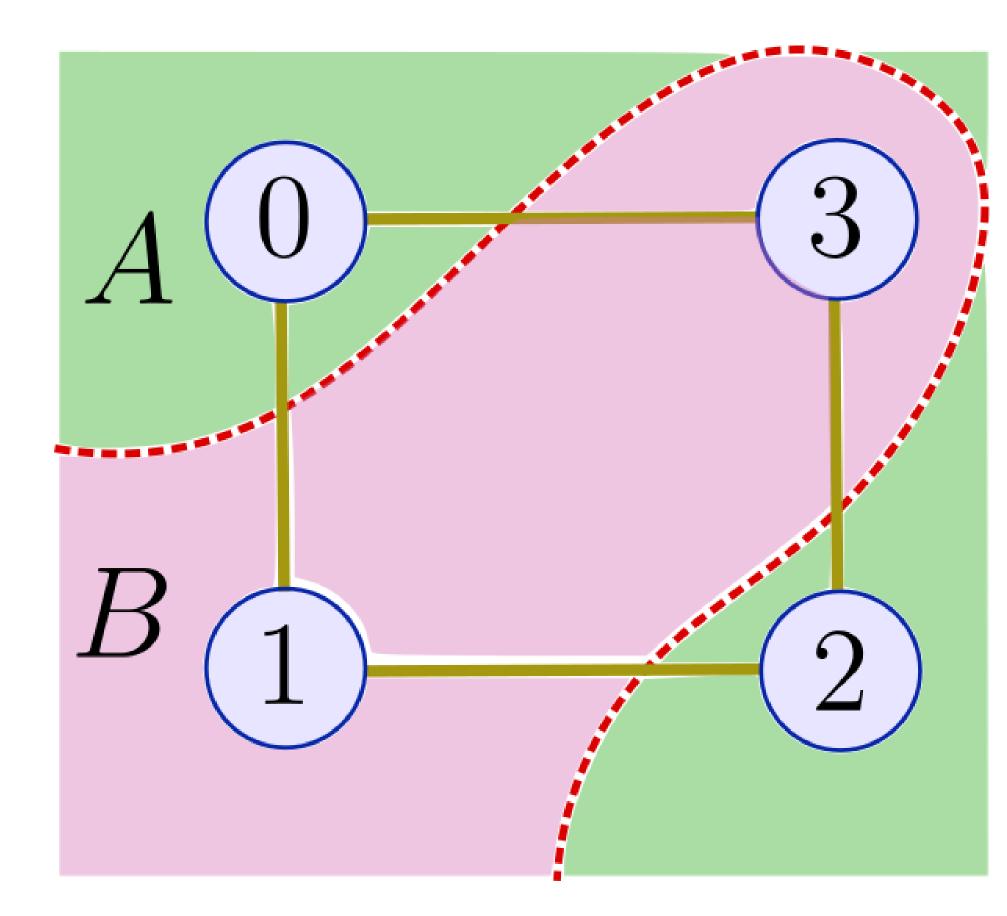
cuTensorNet

Tensor Network path optimization performance

Time to find a contraction path (sec/sample)

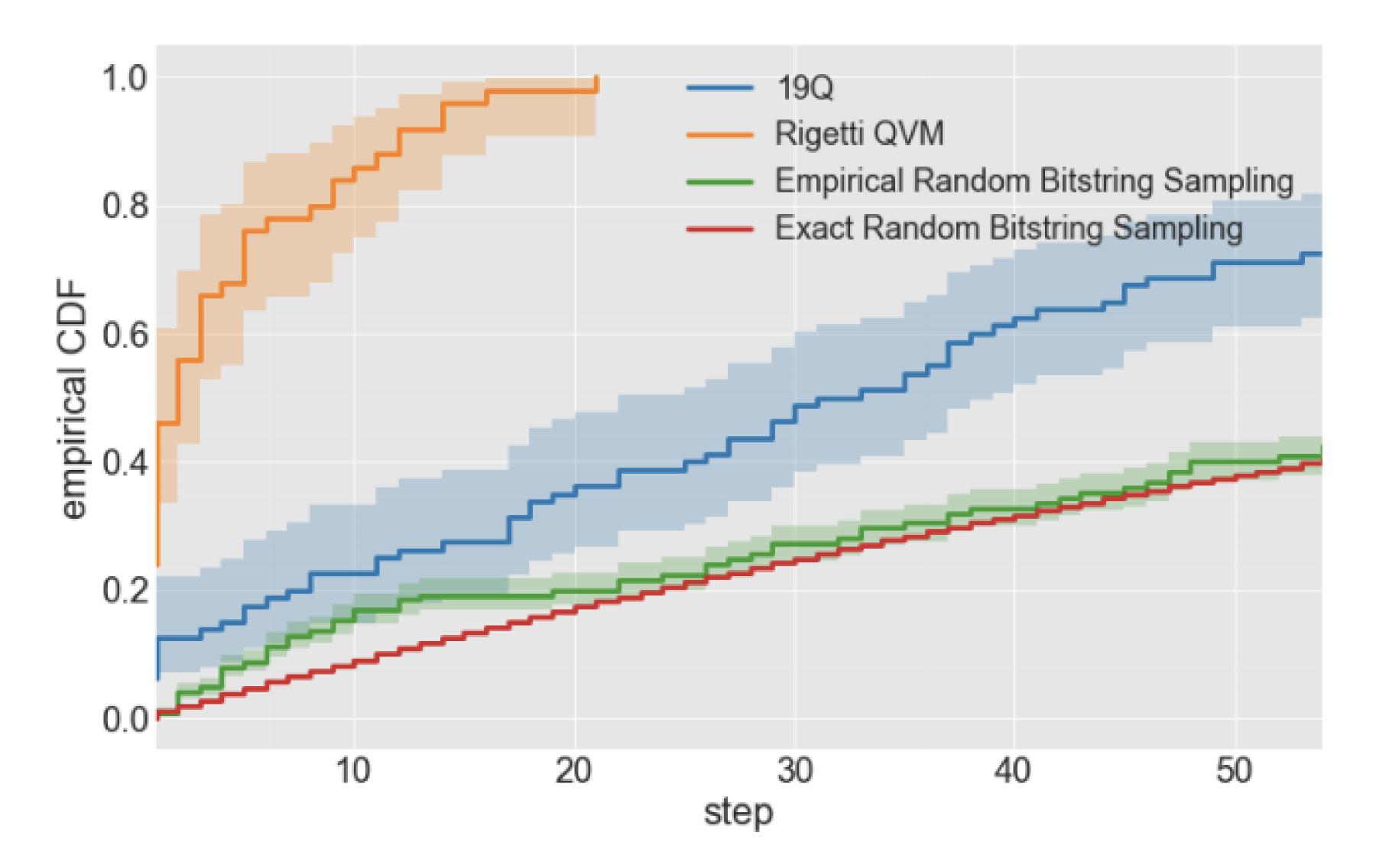
40
40
22461
3316 tensors





- NP-Complete combinatorial optimization problem
- Applications include clustering, network design, Statistical Physics, and more

The MaxCut Problem



- algorithms
- Rigetti 19Q chip in 2017

• Early target for hybrid variational quantum

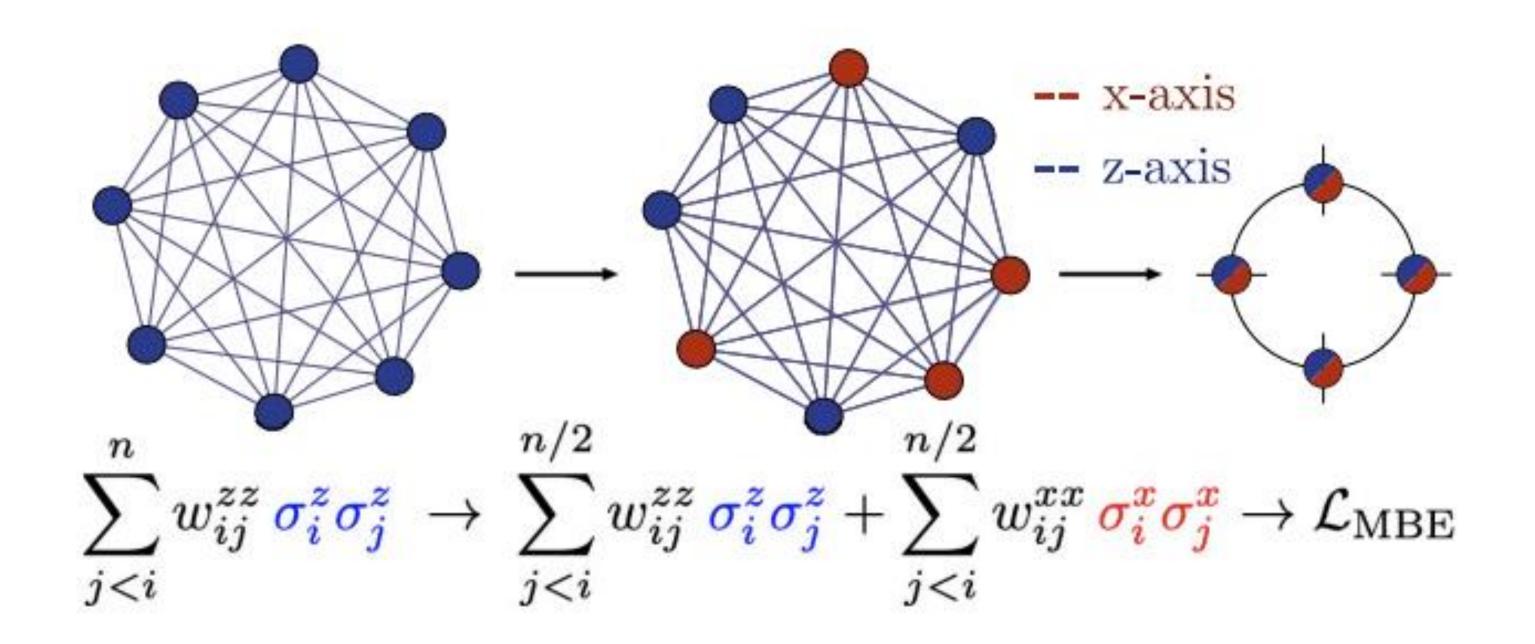
QAOA proposed by Farhi et al: arXiv:1411.4028

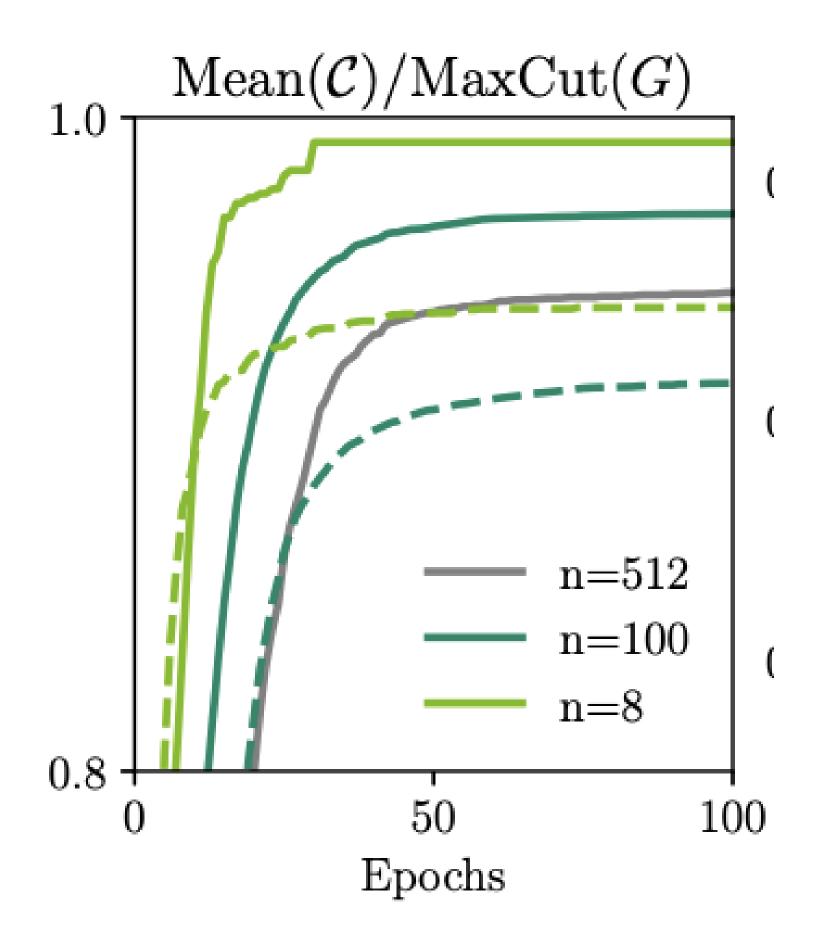
Several HW demonstrations, including on



Simulating MaxCut using Tensor Networks

- Tensor Networks are a natural fit for MaxCut
 - Fried et. al. (2017) <u>arxiv.org/abs/1709.03636</u>
 - Huang et. al (2019) <u>arxiv.org/abs/1909.02559</u>
 - Lykov et. al. (2020) <u>arxiv.org/abs/2012.02430</u>
- Patti et. al.(2021): NVIDIA Research proposes a novel variational quantum algorithm
 - Based on 1D tensor ring representation
 - Multibasis encoding
 - Able to find accurate solution for 512 vertices (256 qubits) on a single GPU
 - Paper: arxiv.org/abs/2106.13304
 - Code: <u>github.com/tensorly/quantum</u>







Scaling to a GPU Supercomputer: NVIDIA DGX SuperPOD

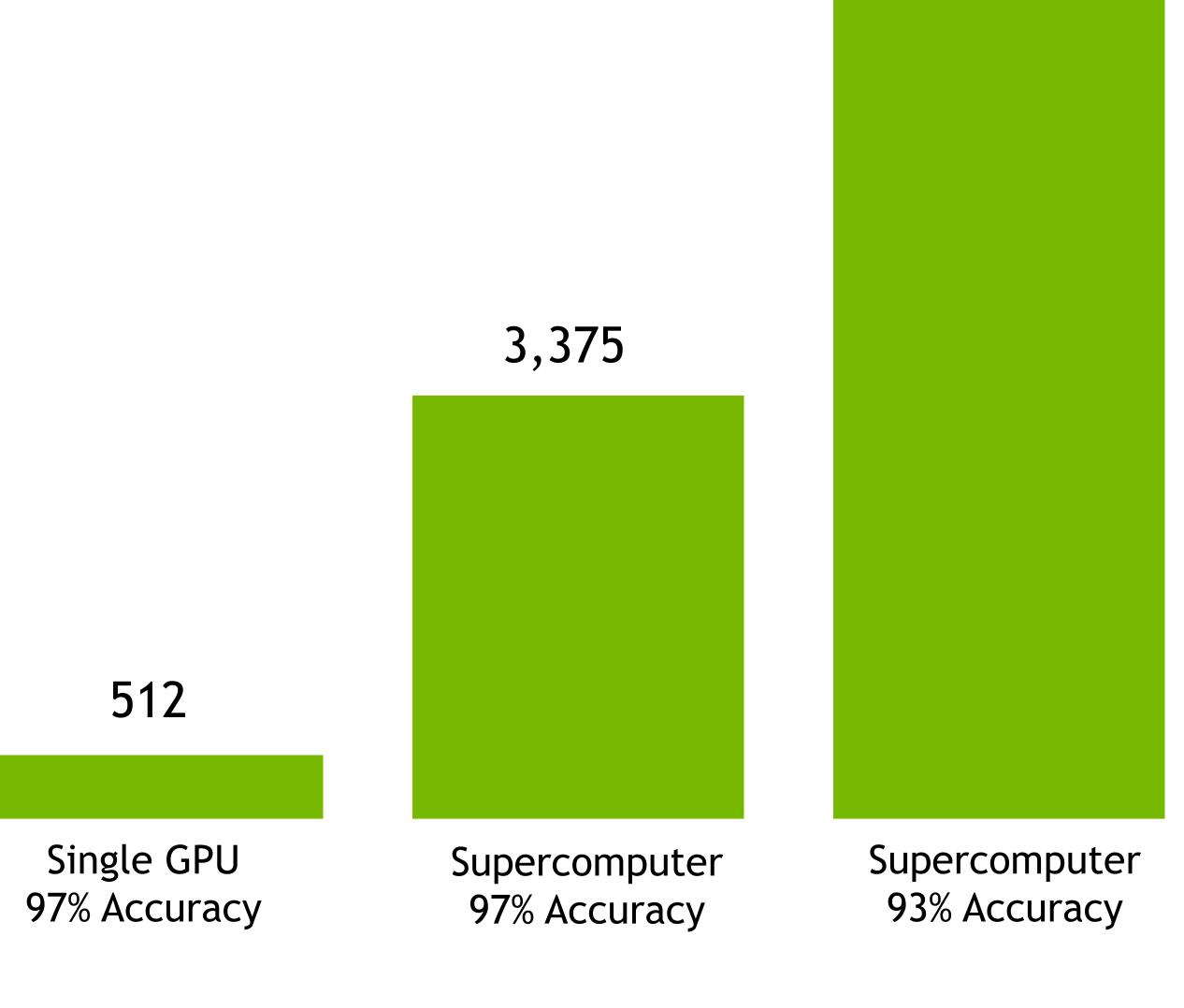


NVIDIA's Selene DGX SuperPOD based supercomputer

- Using NVIDIA's Selene supercomputer
- Solved a 3,375 vertex problem (1,688 qubits) with 97% accuracy
- Solved a 10,000 vertex problem (5,000 qubits) with 93% accuracy

210

Previous largest problem, Theta Supercomputer [1]



arxiv.org/abs/2012.02430

Vertex Count

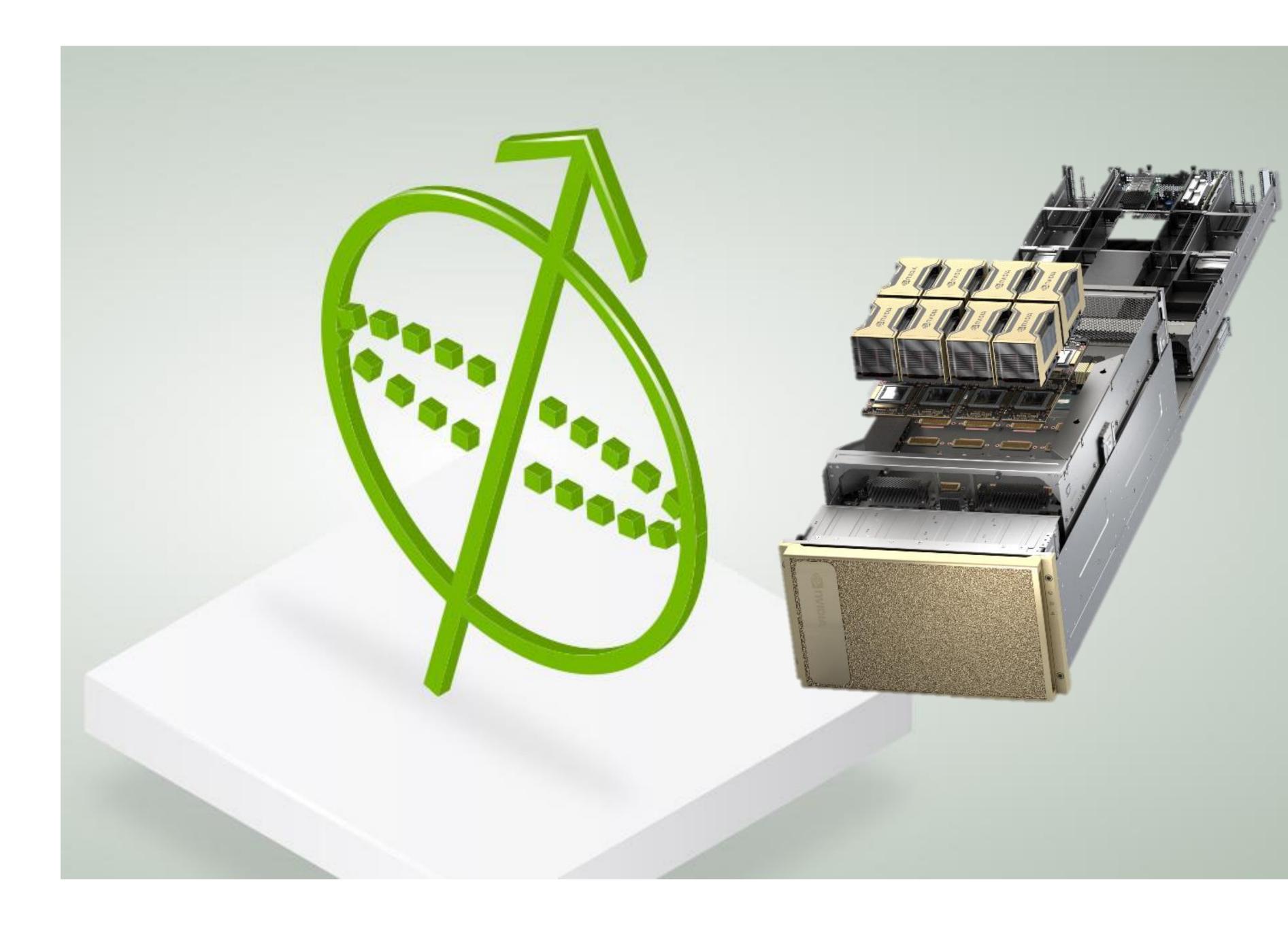
10,000

[1] Danylo Lykov et al, Tensor Network Quantum Simulator With Step-Dependent Parallelization, 2020



- Quantum circuit simulation is an approach to conduct quantum computation with classical computer processors like CPUs and GPUs
- cuQuantum makes it easy for anyone with NVIDIA hardware to accelerate and scale their simulations more than previously possible
- An expanding ecosystem is using cuQuantum to enable quantum research
- Get stated with cuQuantum today by pulling our container from NGC, downloading the SDK from our DevZone, via pip or conda install, or through other frameworks

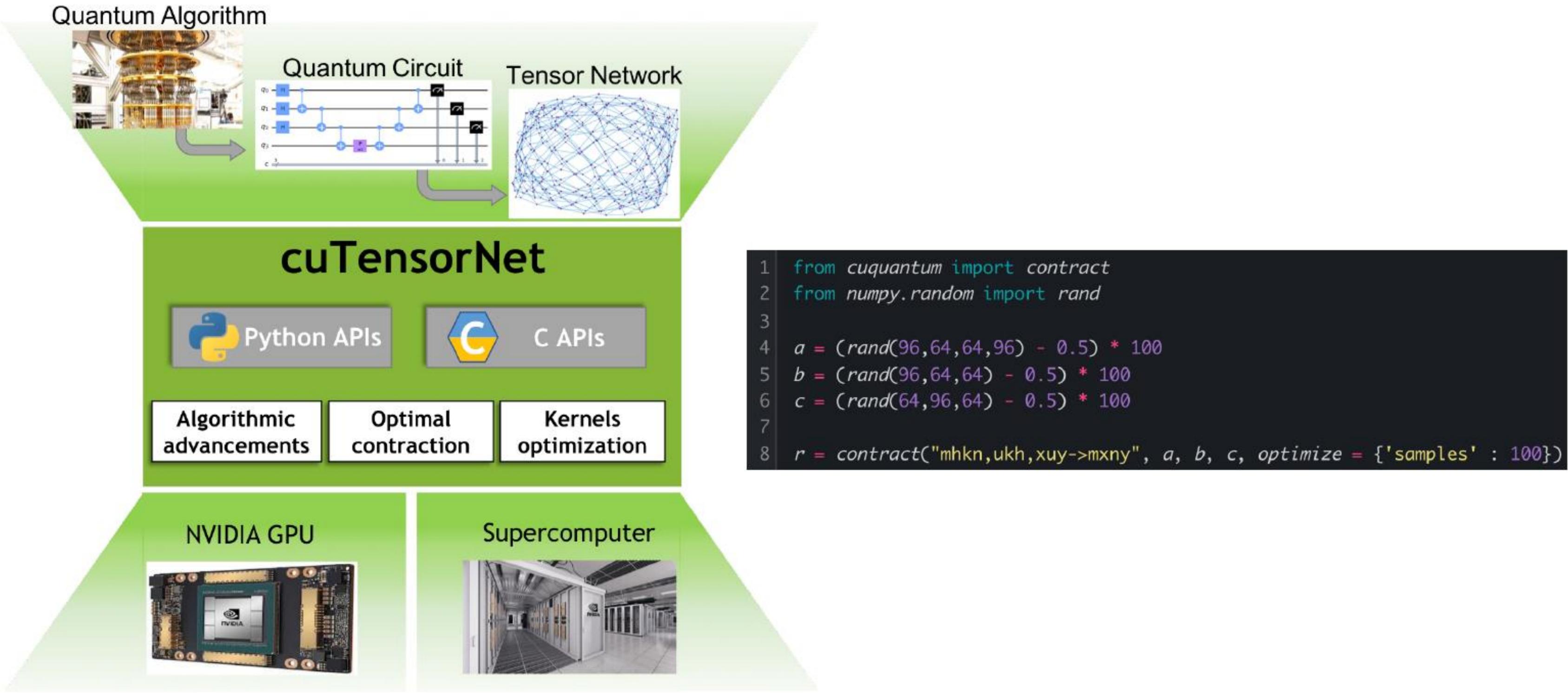
Summary





Tensor Networks & cuTensorNet





cuTensorNet

A library to accelerate Tensor Network based Quantum Circuit simulation

<u>developer.nvidia.com/blog/scaling-quantum-circuit-simulation-with-cutensornet</u>



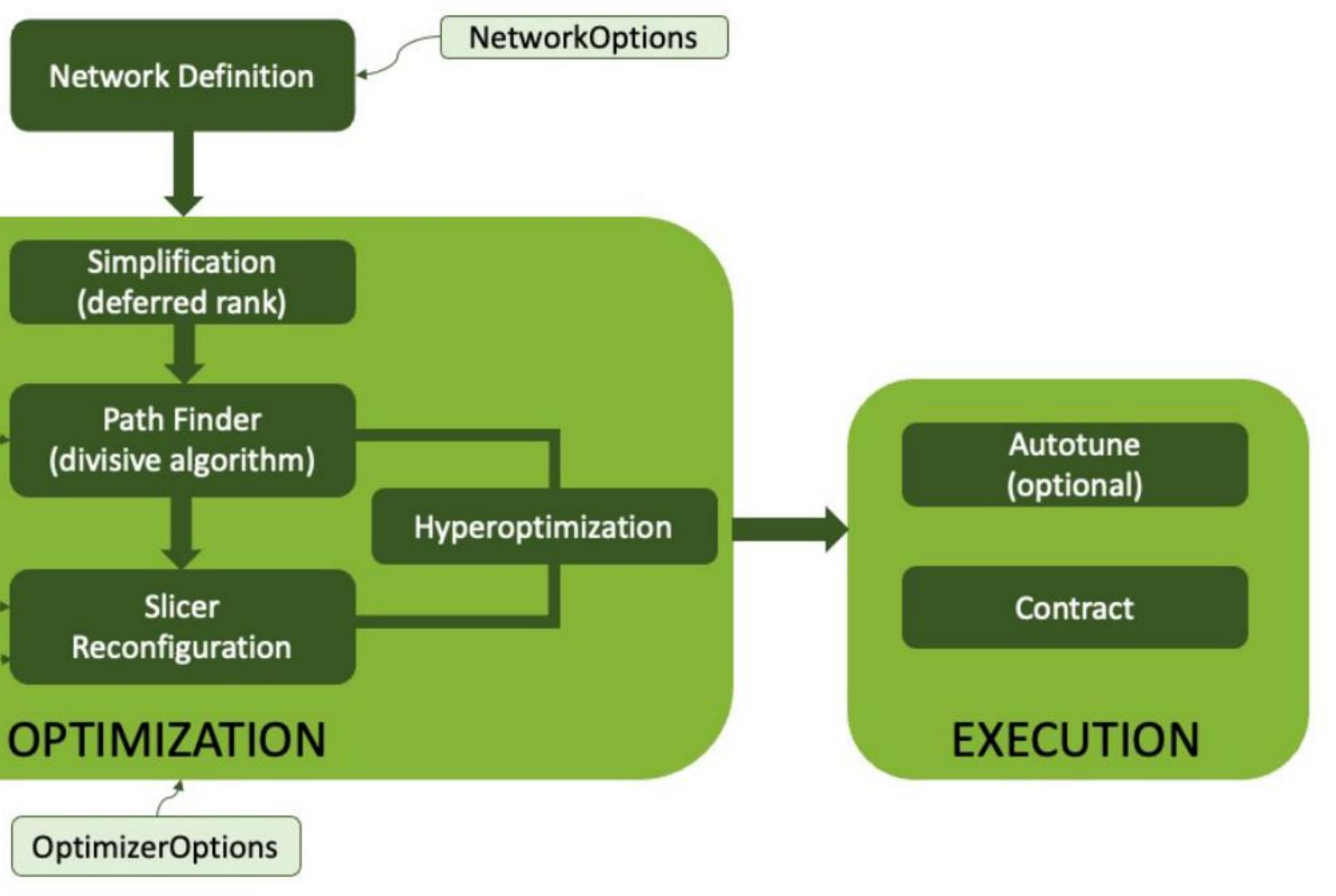
cuTensorNet Optimization & Flowchart

PathFinderOptions

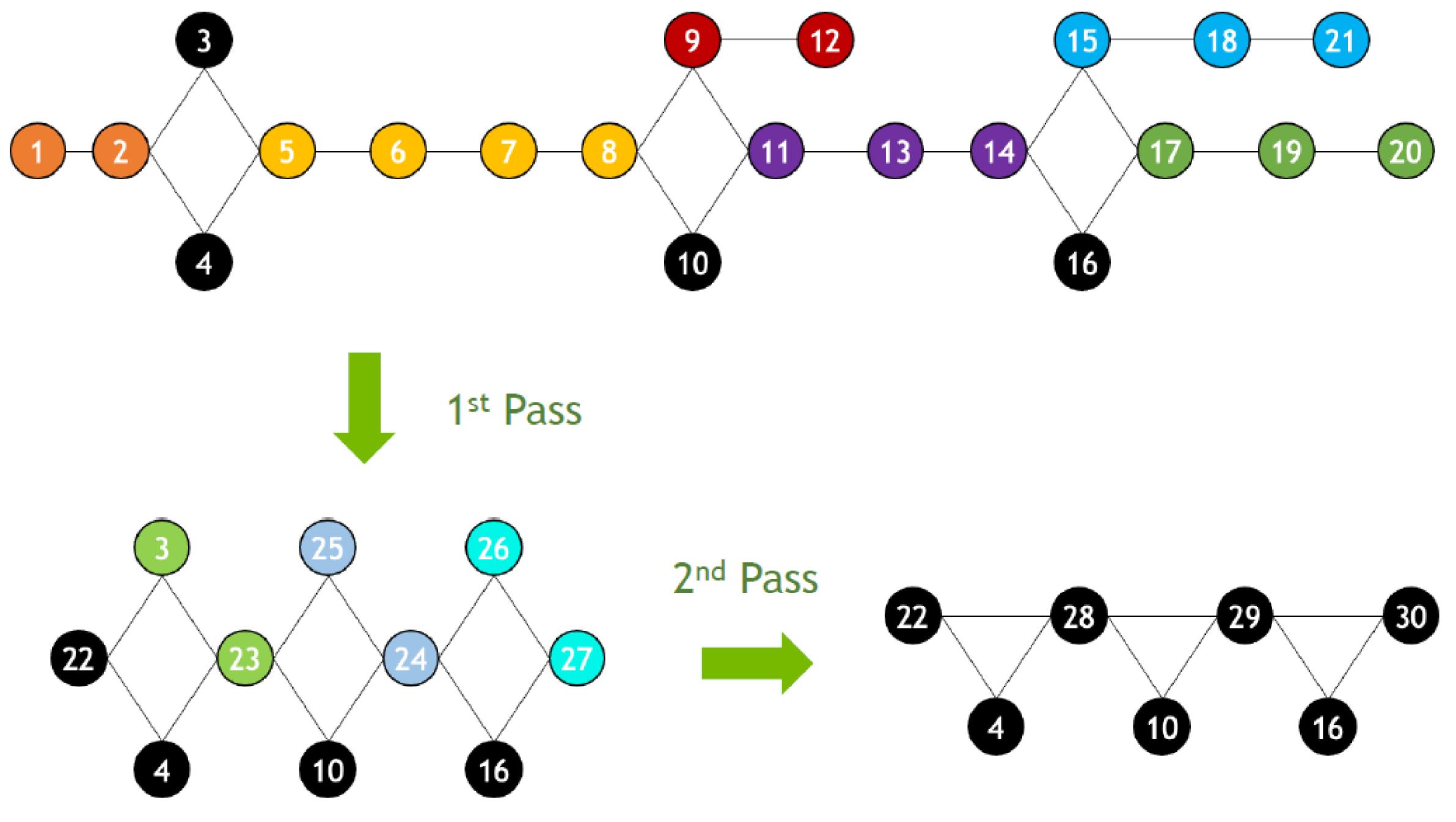
SlicerOptions

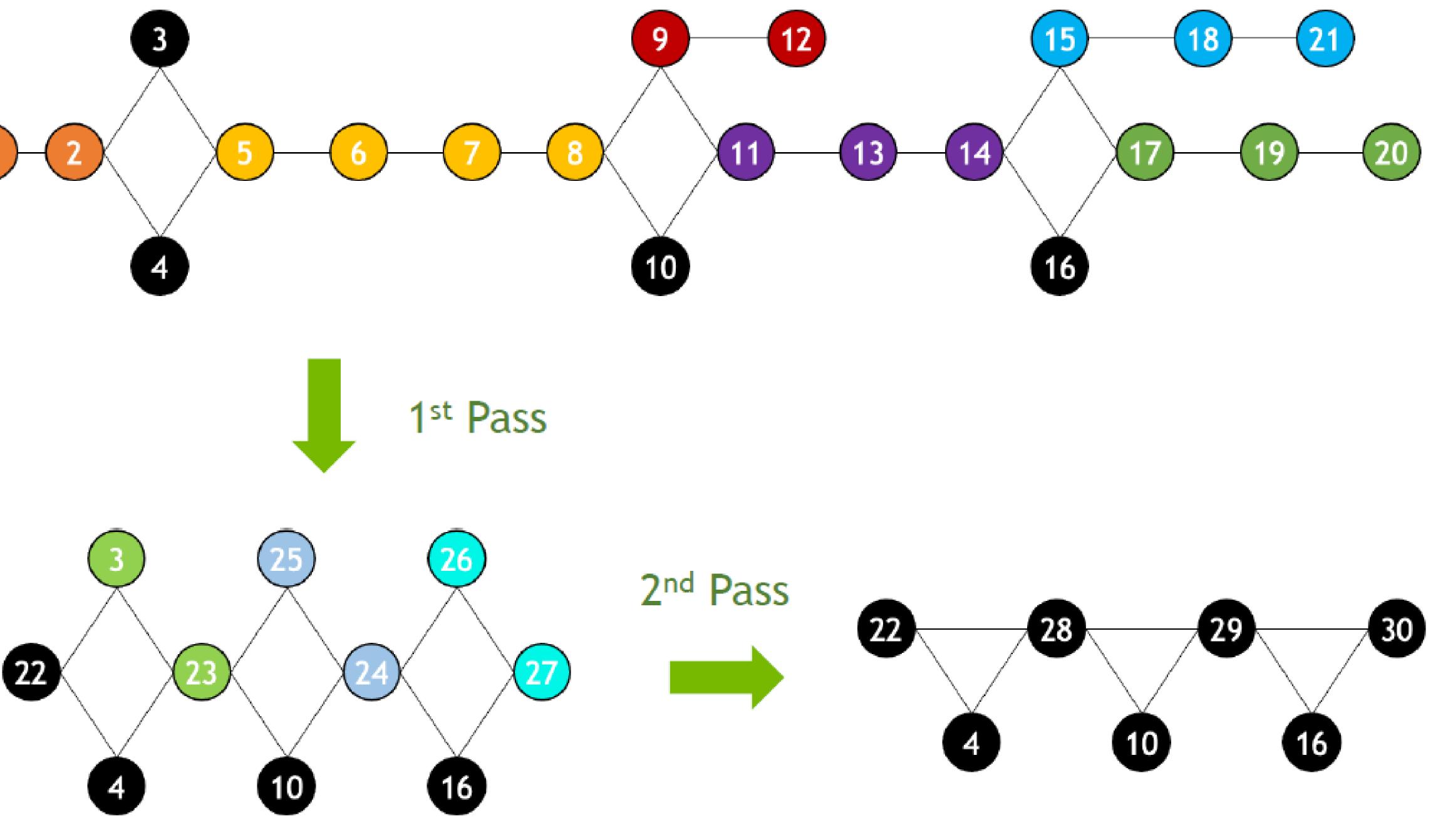
ReconfigOptions











Tensor Network Simplification

• Simplification aims to reduce the computational cost of contracting the tensor network through preprocessing.

• cuTensorNet implements deferred rank-simplification, which identifies those pairwise contractions that do not increase the rank (number of dimensions) of the resulting tensor and sequences them to be performed first as a path prefix. This essentially creates a smaller network for the divisive algorithm as well as for reconfiguration to process.



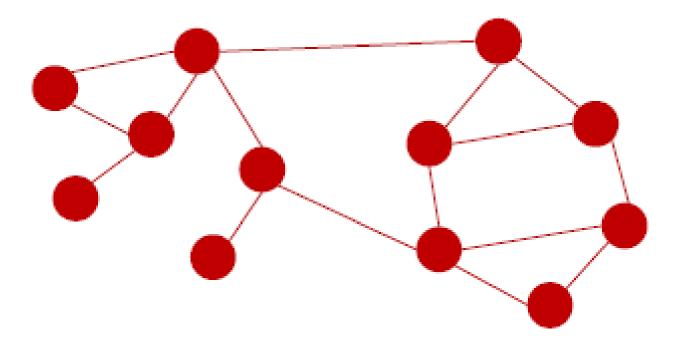
cuTensorNet Path Finder (Divisive Algorithm)

edges.

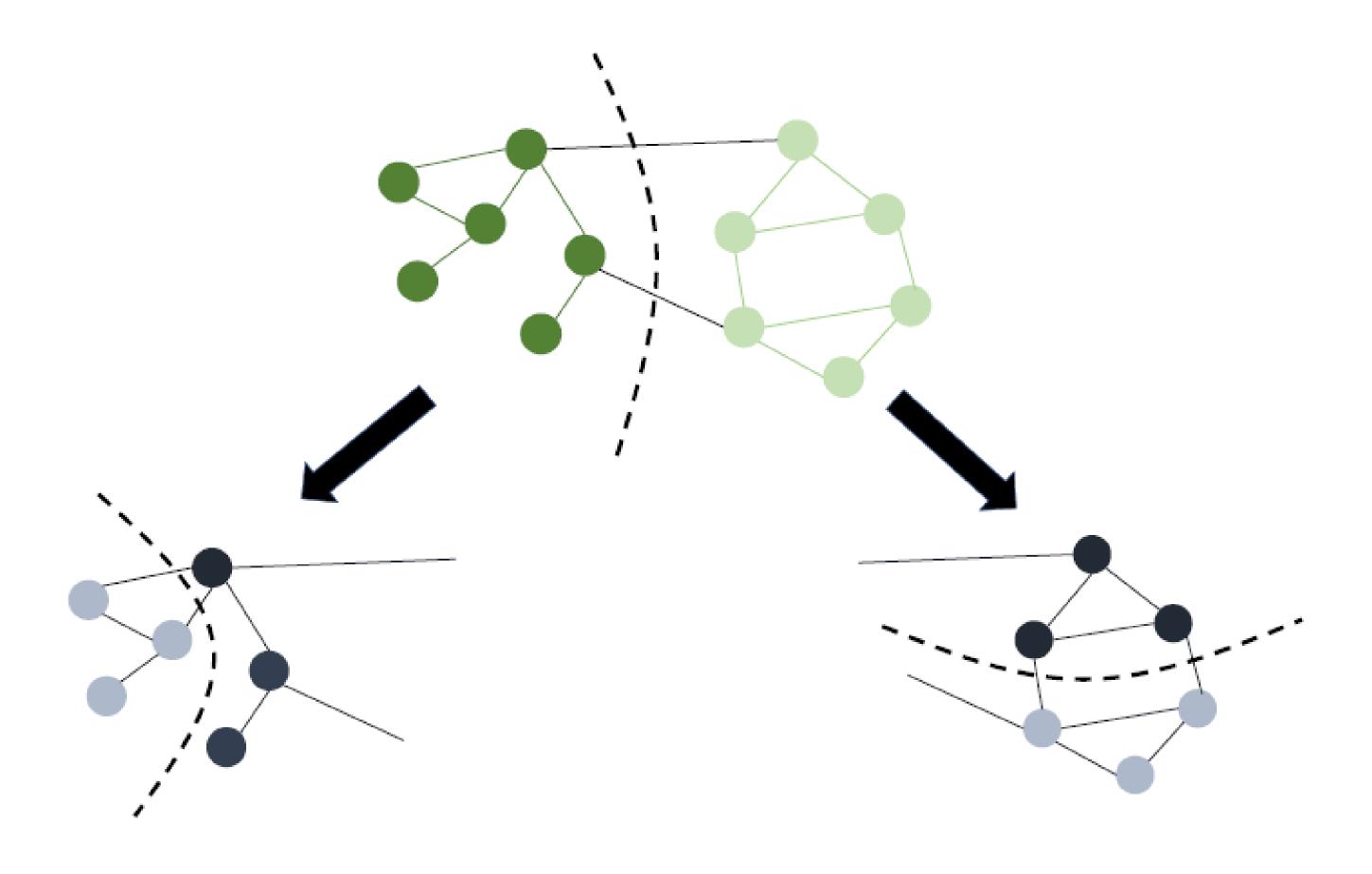
tensor network is built.

The colors map to the partitioning level, and the shades at each level distinguish different partitions.

• The tensor network is represented as a graph, with tensors as the vertices and modes that are contracted as the



• The graph is partitioned into the specified number of partitions (2 shown) recursively until the size of each partition is less than or equal to the specified cutoff size (3 shown). Exhaustive search or an agglomerative algorithm is used to find the contraction order within as well as between partitions, from which the contraction order for the complete



Level 1

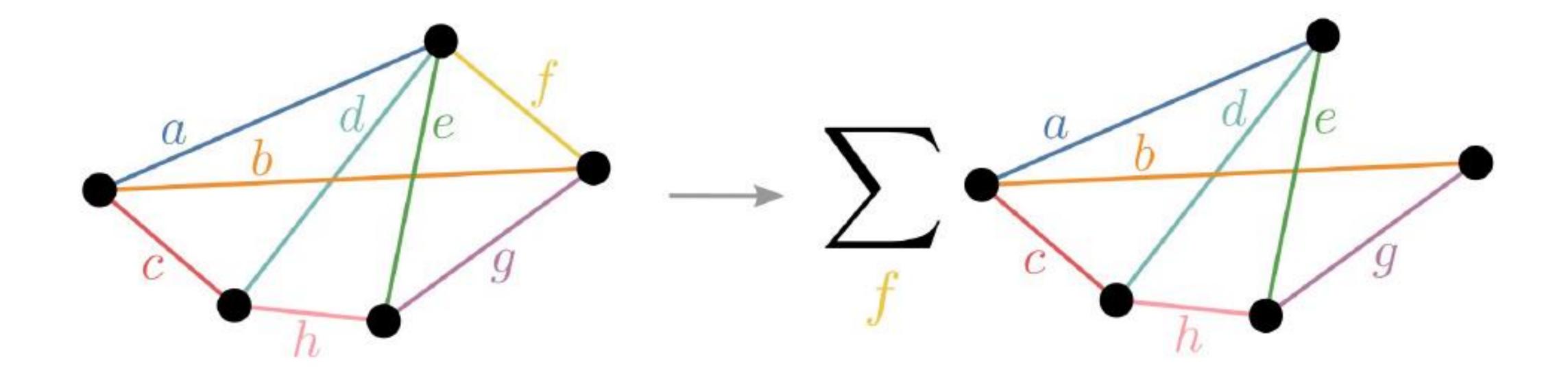
Level 2



Tensor Network Slicing for Parallelism & Minimizing Memory Requirements

- summation.
- A sliced network:

 - 2. allows for parallel execution.



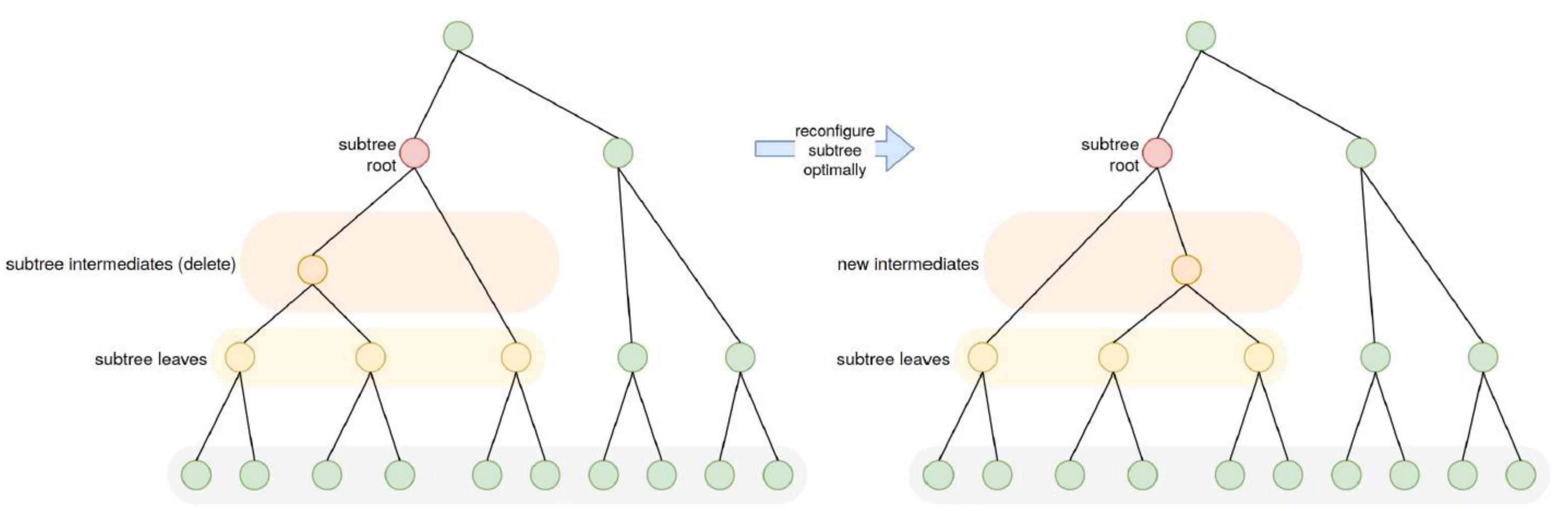
• Slicing is a technique to select a subset of edges from a tensor network (corresponding to mode labels) for explicit

• 1. results in lower memory requirements (often with some computational overhead), and

• cuTensorNet implements dynamic slicing, which interleaves slicing with reconfiguration.



- cost low.



original tensors (real tree leaves)

Tensor Network Reconfiguration

• The divisive algorithm computes a contraction path, which is a linearization of the contraction tree. The basic idea behind reconfiguration is to reduce the total contraction cost by reducing the contraction cost of portions (subtrees) of the contraction tree. The number of leaves in the subtree is typically chosen to be small enough so that the optimal algorithm can be used, and multiple iterations of reconfiguration are performed on different subtrees.

• As mentioned earlier, if slicing is active cuTensorNet interleaves reconfiguration with slicing to keep the contraction

original tensors (real tree leaves)



Demo 4: VQE circuit with cuTensorNet



Demo 5: M10 Sycamore circuit





NVIDIA QODA



- cuQuantum SDK web page with download and conda install: <u>developer.nvidia.com/cuquantum-sdk</u> DGX Quantum Appliance container available on NGC (<u>ngc.nvidia.com</u>): • <u>catalog.ngc.nvidia.com/orgs/nvidia/containers/cuquantum-appliance</u>
- - includes Cirq and Qsim
- New PennyLane simulator *lightning.gpu* with cuQuantum support, available now from Xanadu:
 - xanadu.ai/products/lightning
- Full documentation at <u>docs.nvidia.com/cuda/cuquantum</u>
- cuStateVec technical article on NVIDIA Devblog:
 - <u>developer.nvidia.com/blog/accelerating-quantum-circuit-simulation-with-nvidia-cuStateVec</u>
- cuTensorNet technical article on NVIDIA Devblog:
 - <u>developer.nvidia.com/blog/scaling-quantum-circuit-simulation-with-cutensornet</u>
- Tensor Network contraction optimization paper:
 - Johnnie Gray and Stefanos Kourtis, <u>"Hyper-optimized tensor network contraction</u>", Quantum, volume 5, 2021.
- What is a QPU? <u>blogs.nvidia.com/blog/2022/07/29/what-is-a-qpu</u>
- NVIDIA QODA: <u>developer.nvidia.com/qoda</u>
- QODA technical article on NVIDIA Devblog:
 - <u>developer.nvidia.com/blog/introducing-qoda-the-platform-for-hybrid-quantum-classical-computing</u>

Useful References









Thank you

cnardone @ nvidia.com ahehn @ nvidia.com zchandani @ nvidia.com andrea.pasquale @ unimi.it stavros.efthymiou @ tii.ae

