QILIMANJARO QUANTUM · TECH

A coherent Quantum annelaer on the cloud

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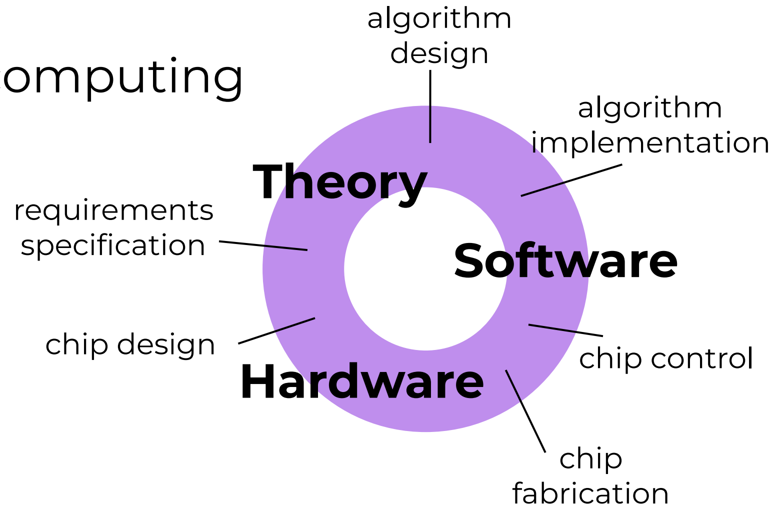
0. What Qilimanjaro is up to

- Start-up focused on analog quantum computing
- Aimed at maximum THS integration
- Coherent superconducting flux qubits
- Aimed at going beyond Ising model
- Partners in AVaQus



- Spin-off from:

BSC Barcelona Supercomputing Center
Centro Nacional de Supercomputación

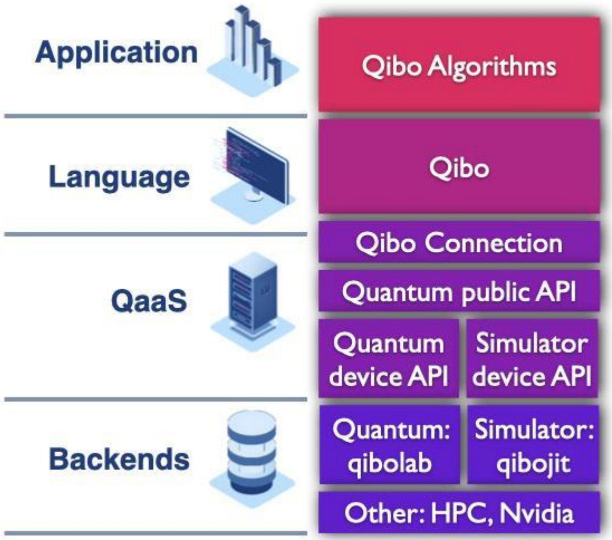
IFAE
Institut de Física d'Altes Energies

UNIVERSITAT DE BARCELONA

0. What Qilimanjaro's *HW and SW* teams are up to

Software

- Qilimanjaro SW services layout



Qibo: https://qibo.science/

Hardware

- Design, fabrication and characterization of superconducting qubit technology

0. What Qilimanjaro's *theory team* is up to

Innovation

- Fundamental theory of annealing
- New algorithms and encodings
- Hybrid strategies with an analog system

Applications

- Consultancy on quantum state of the art
- Formulation of algorithms tailored to customer's problems with existing know-how

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Internal bridge with hardware and software

- Theory behind the hardware
- Algorithm integration, compilation and optimisation

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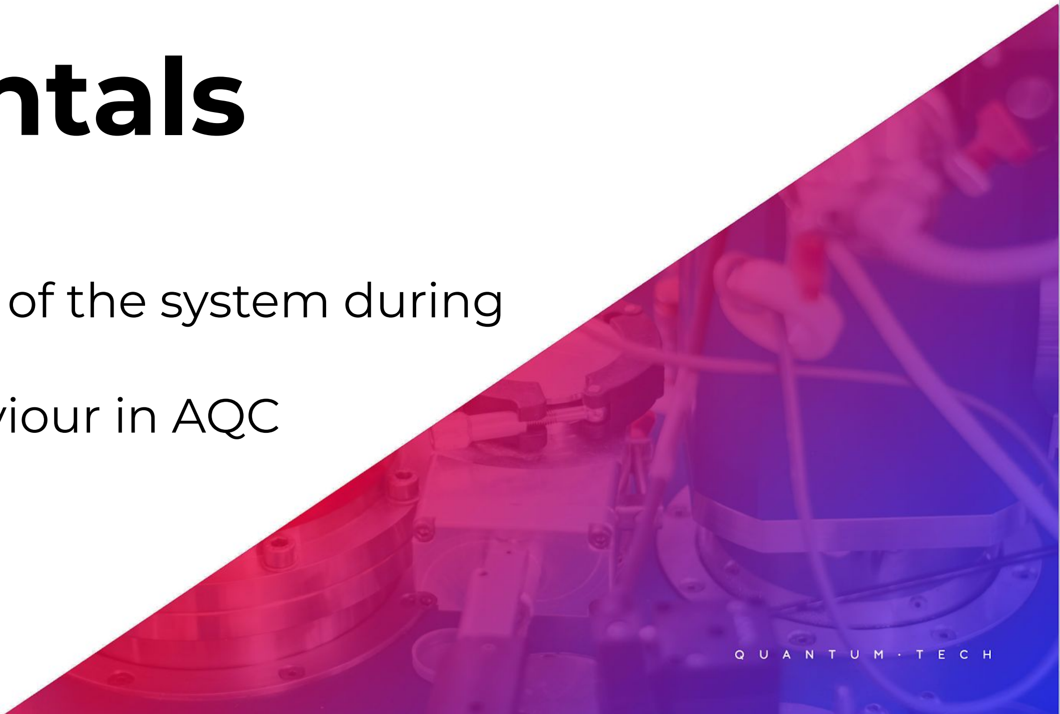
1. Fundamentals

- Understand behaviour of the system during the annealing process
- Understand gap behaviour in AQC

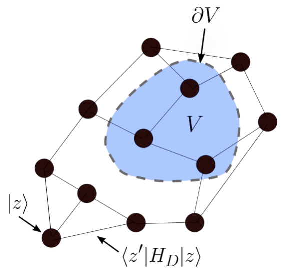


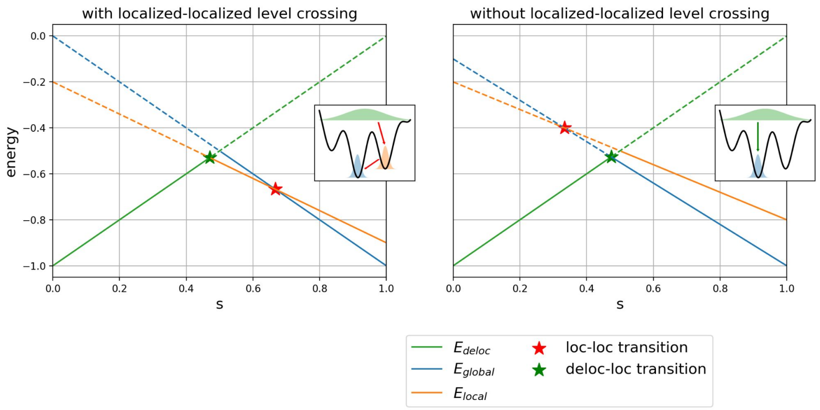
1. Fundamentals.–

Graph-theoretical analysis on 1st order QPTs for AQC

- Driver (+catalyst) Hamiltonian analysed from graph theory perspective to study loc-loc vs. deloc-loc transitions
- New results on the incorporation of stoquastic/nonstoquastic catalysts

$$\frac{d_{max}(V)}{d_{max}(V)+d\Delta E_T} \leq s \leq \frac{1-\frac{\phi(V)}{d}}{1-\frac{\phi(V)}{d}+\Delta E_T}$$





1. Fundamentals.– Steered QA

arXiv:2206.07646
(to be updated)

Improve time efficiency of AQC algorithm with partial information

$$H_0^{std} = -\sum_i^N \sigma_i^x$$

$$H_0 = R_y^\dagger(\vec{\theta}) H_0^{std} R_y(\vec{\theta}) = \sum_i^N -[\cos(\theta_i)\sigma_i^x + \sin(\theta_i)\sigma_i^z]$$

Control over confidence in assignment

$$\vec{\theta} = \Theta\vec{\psi}$$

recommendation / assignment / guess

$$\psi_i = \begin{cases} +1(-1) & \text{if spin } i \text{ is assigned upwards (downwards)} \\ 0 & \text{if there is no information on spin } i \end{cases}$$

Similar proposals: Graß, PRL 123 (2019); arXiv:2205.15820

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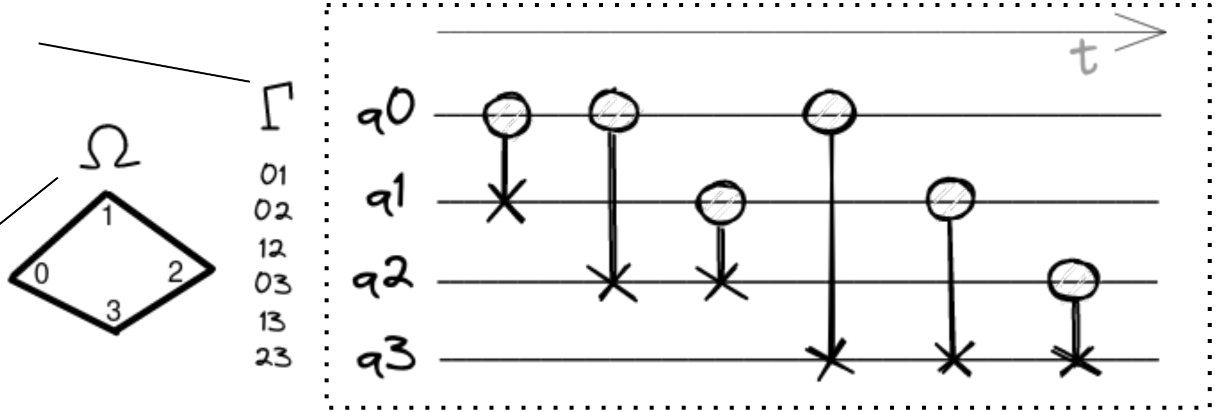
2. Resource-efficient encodings

- Need to optimise required resources if we want to tackle large problems with significantly less qubits than those required by a fault-tolerant computer

2. Resource-efficient encodings.– An *heuristic* algorithm for qubit allocation

Instruction set

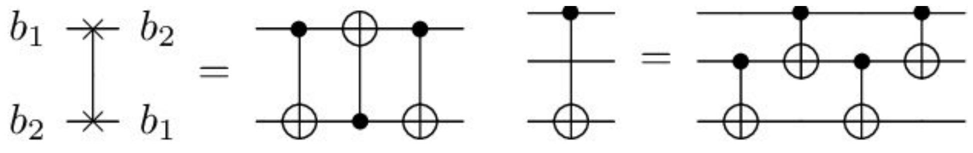
Hardware connectivity



Ideal realisation of the instruction set

not feasible

Need to add extra gates

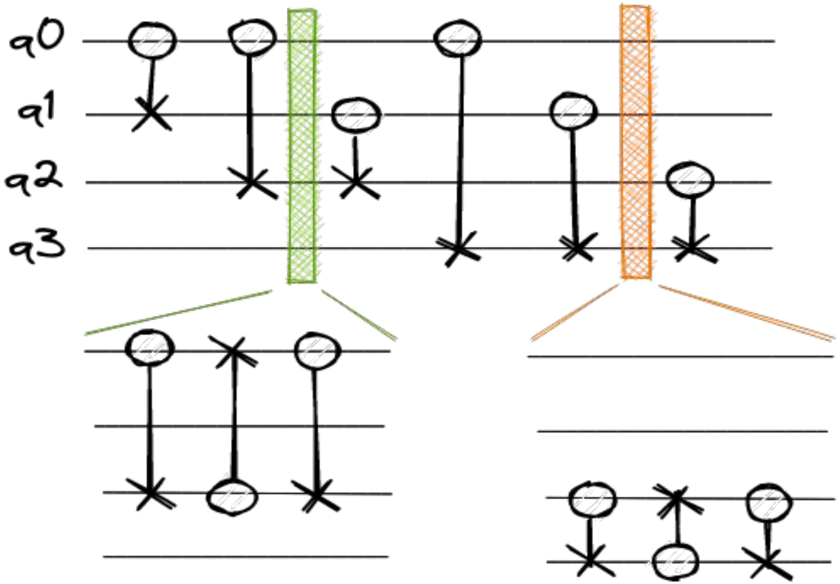


(a) SWAP gate

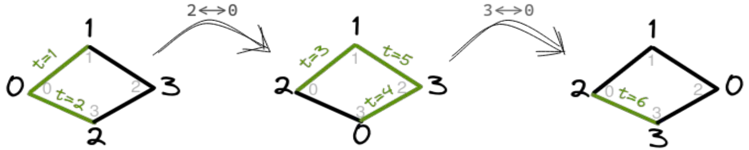
(b) Bridge gate

- Image from T. Itoko et al., *Optimization of quantum circuit mapping using gate transformation and commutation* (2020)

2. Resource-efficient encodings.– An *heuristic* algorithm for qubit allocation



Good solution



- Longer computation
- Increased error

Full solution:
Initial allocation + set of transformations

2. Resource-efficient encodings.– An *heuristic* algorithm for qubit allocation

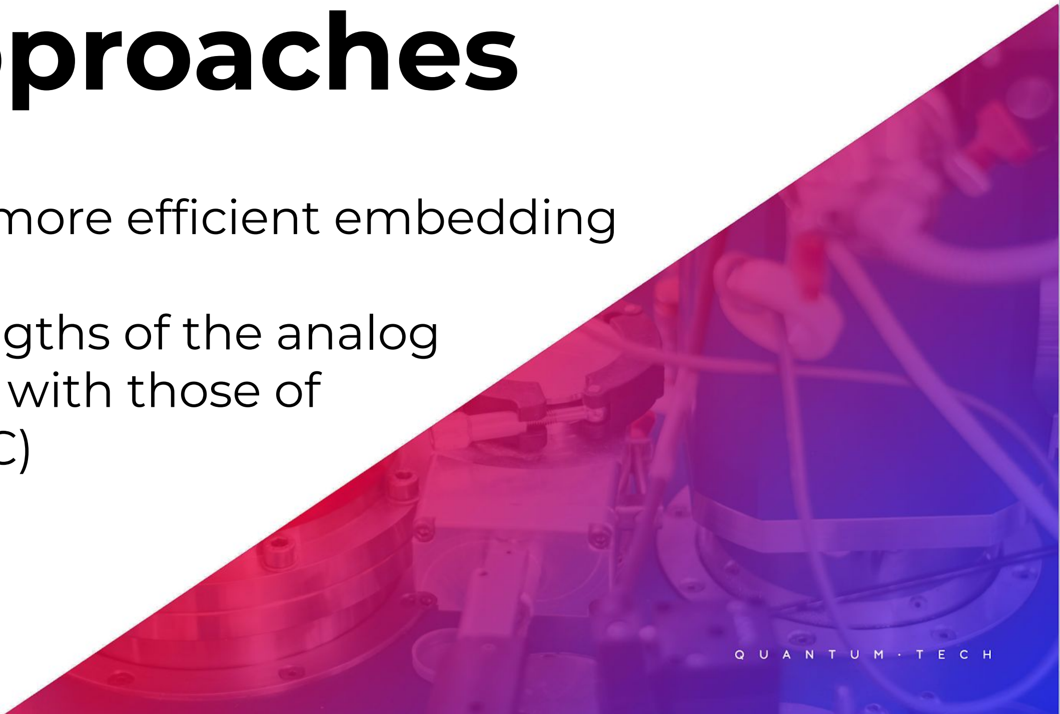
Does not provide an exact solution, but only a heuristic (at least for non-shallow circuits)

- Dim of the exploited Hilbert space is $d_{H,eff}^{alg} = L_v N!$
- Dim of qubit allocation is hard to assess due to dependence on problem instance, but on a rough estimate $d_H^{simp} = [\alpha(N)]^{L_v}$

$$n_{min}^{alg} = N \log_2 N + \log_2 L_v \qquad\qquad n_{min}^{simp} = L_v \log_2 \alpha(N)$$

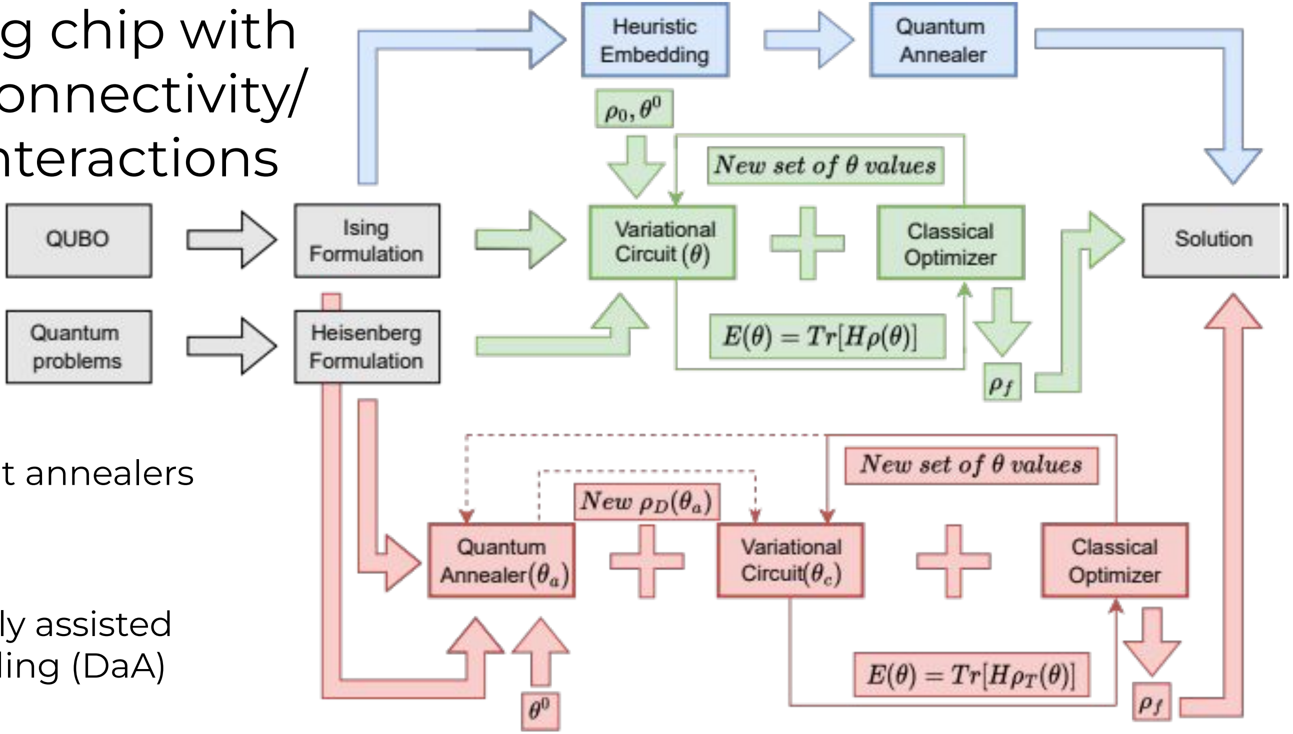
3. Hybrid approaches

- Search for alternative, more efficient embedding schemes
- Complement the strengths of the analog model of computation with those of other models (GM, QRC)



3. Hybrid approaches.– Embedding strategies for AQC

- Annealing chip with limited connectivity/ limited interactions



Current annealers

VQE

Digitally assisted Annealing (DaA)

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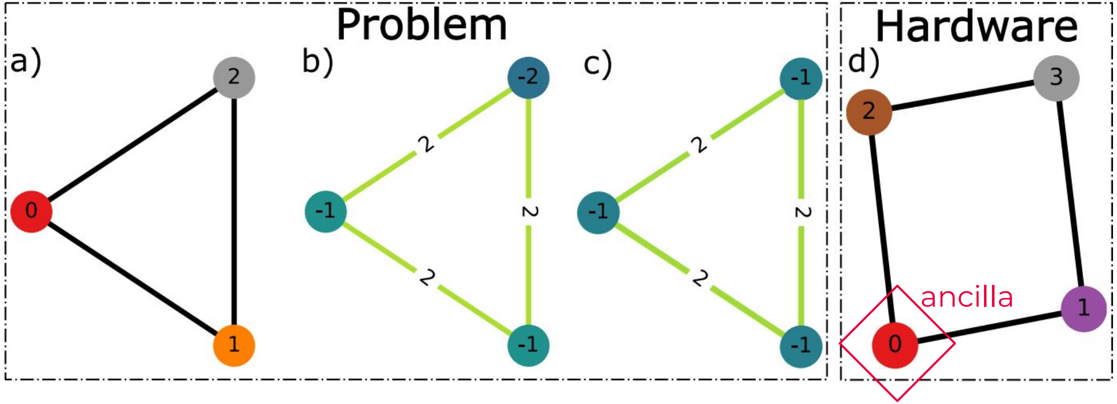

Target graph Unique GS Degenerate GS **HW graph**

Ising/Heisenberg Ising

Somewhat noisy annealer chip prepares Gibbs state at some effective temperature T

$$\rho_D = \frac{1}{Z} e^{-\frac{H_D(\theta')}{K_B T}}$$

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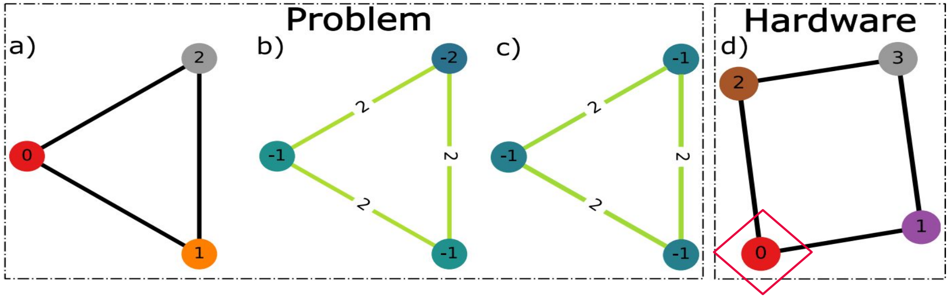

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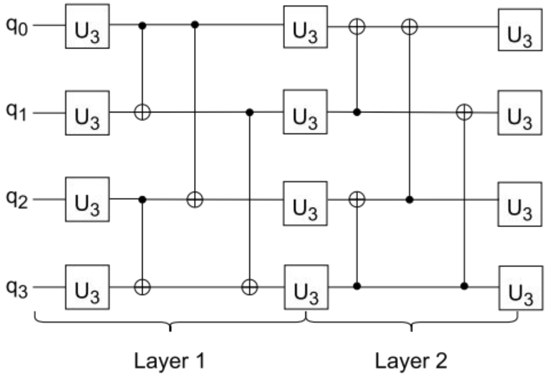
Apply parametrised circuit *U*(θ) (layers respect device connectivity)



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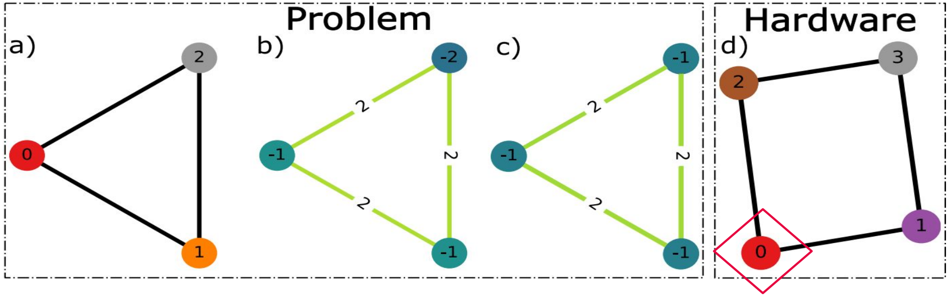


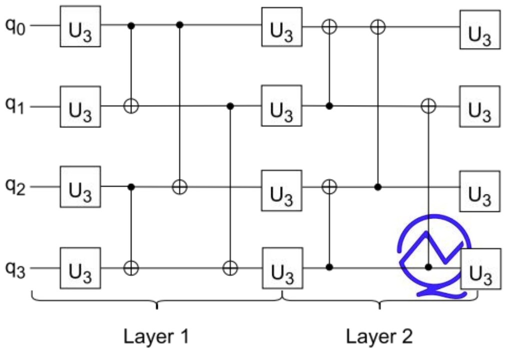
Somewhat noisy annealer chip prepares Gibbs state at some effective temperature T

$$\rho_D = \frac{1}{Z} e^{-\frac{H_D(\theta')}{K_B T}}$$

Compute cost function and update parameters

$$C = \mathrm{Tr}[\mathrm{Tr}_A \left(U \rho_D U^{\dagger}\right) H_{target}]$$

Apply parametrised circuit $U(\theta)$ (layers respect device connectivity)



- Cerezo, M. et al. *Variational quantum state eigensolver*. npj Quantum Inf 8, 113 (2022)

VQSE

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